Finisar

Product Specification

2.5Gb/s Active Copper GBIC Transceiver

FCM-8520-2-2.5

Finisar's FCM-8520-2-2.5 2.5Gb/s copper GBIC transceivers comply with GBIC Specification Revision 5.4[1]. They are compatible with the Gigabit Ethernet 1000BASE-CX standard as specified in IEEE Draft P802.3z/D5.0[2] and with Fibre Channel FC-PH3[3] and FC-PI 7.4[4]. The modules are supplied with an HSSDC connector. They are 3.3V and 5V compatible.

I. GBIC to Host Connector Pin Out

Pin Name	Pin #	Sequence
RX_LOS	1	2
GND	2	2
GND	3	2
MOD_DEF(0)	4	2
MOD_DEF(1)	5	2
MOD_DEF(2)	6	2
TX_DISABLE	7	2
GND	8	2
GND	9	2
TX_FAULT	10	2
GND	11	1
-RX_DAT	12	1
+RX_DAT	13	1
GND	14	1
V_{CC}	15	2
V_{CC}	16	2
GND	17	1
+TX_DAT	18	1
-TX_DAT	19	1
GND	20	1

Table 1. GBIC to host connector pin assignment

"Sequence" indicates the order in which pins make contact when the device is hot plugged.

Also see "Table 3: Signal Definitions" in the GBIC Specification Revision 5.4.[1]

II. +5/3.3 Volt Electrical Power Interface

Finisar copper GBICs have an extended power supply voltage range of 3.00V to 5.5V as described in Table 2. The GBIC specification calls for a range of 4.75V to 5.25 volts. The 6V maximum voltage is not allowed for continuous operation, however, TX_DISABLE circuitry in Finisar copper GBICs will function at 6V.

+5/3.3 Volt Electrical Power Interface

Parameter	Symbol	Min	Typ	Max	Units	Notes/Conditions
Supply Current	I_s		140	180	mA	Preliminary
Maximum Voltage	V_{max}			6	V	
Surge Current	I_{surge}			+30	mA	Hot plug, above steady state current.
Input Voltage	V_{cc}	3.00	3.3, 5	5.5	V	Referenced to GND. 3.3V and 5V compatible

Table 2. +5/3.3 volt electrical power interface

III. Low Speed Signals

Pin Name	Pin #	Description	Pin Name	Pin #	Description
RX_LOS	1	Receiver Loss of Signal CMOS Open Drain Output	RGND	11	GND
RGND	2	GND	-RX_DAT	12	-RX
RGND	3	GND	+RX_DAT	13	+RX
MOD_DEF(0)	4	TTL LOW (Tied to GND)	RGND	14	GND
MOD_DEF(1)	5	SCL CMOS Open Drain Serial Clock	VDDR	15	VCC
MOD_DEF(2)	6	SDA CMOS Open Drain Serial Data	VDDT	16	VCC
TX_DISABLE	7	Transmitter Disable, TTL Input	TGND	17	GND
TGND	8	GND	+TX_DAT	18	+TX
TGND	9	GND	-TX_DAT	19	-TX
TX_FAULT	10	TTL LOW (Tied to GND) - TX_FAULT Not Implemented	TGND	20	GND

Table 3. GBIC pin usage, HSSDC copper modules

Low Speed Signals, Electronic Characteristics					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes/Conditions**
GBIC Output LOW	V_{OL}	0	0.5	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector
GBIC Output HIGH	V_{OH}	host_Vcc - 0.5	host_Vcc + 0.3	V	4.7k to 10k pull-up to host_Vcc, measured at host side of connector
GBIC Input LOW	V_{IL}	0	0.8	V	4.7k to 10k pull-up to Vcc, measured at GBIC side of connector
GBIC Input HIGH	V_{IH}	2	Vcc + 0.3	V	4.7k to 10k pull-up to Vcc, measured at GBIC side of connector

*Note V_{IH} and V_{IL} are the same for both 5V and 3.3V operation

Table 4. Low speed signals – electronic characteristics

Low Speed Signal Parameters						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
RX_LOS Assert Level	--		50		mV	
RX_LOS Deassert Level	--		70		mV	
RX_LOS Hysteresis	--		20		mV	
RX_LOS Assert Delay	t_loss_on		10	100	µsec	From detection of loss of signal to assertion of RX_LOS
RX_LOS Negate Delay	t_loss_off		10	100	µsec	From detection of presence of signal to negation of RX_LOS
TX_DISABLE Assert Time	t_off		5	10	µsec	Rising edge of TX_DISABLE to fall of output signal below 10% of nominal
TX_DISABLE Negate Time	t_on		5	1000	µsec	Falling edge of TX_DISABLE to rise of output signal above 90% of nominal
TX Output Amplitude, TX_DISABLE Asserted				150	mV	Peak to peak

Table 5. Low speed signal parameters (preliminary)

TX_DISABLE is a TTL signal as described in Tables 3 and 4. RX_LOS is a CMOS open drain output. MOD_DEF(1) (SCL) and MOD_DEF(2) (SDA) are open drain CMOS signals (see section VII, "Serial Communication Protocol"). Note that all Finisar copper GBICS are 'module definition 4' since they support the serial identification protocol. MOD_DEF(1), MOD_DEF(2), and RX_LOS must be pulled up to host_Vcc. If host_Vcc is 3.3V, then they must be pulled to 3.3V. If host_Vcc is 3.3V, do not pull the MOD_DEF pins or RX_LOS to 5V. TX_FAULT is not implemented in Finisar copper GBICs.

For more detailed information, see sections 5.3.1 – 5.3.8 in the GBIC Specification Rev. 5.4[1].

IV. High Speed Electrical Interface

All high-speed PECL signals to and from the host board are AC coupled internally.

High Speed Electrical Host – GBIC Interface						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
Data Input Voltage From Host Board to GBIC	V_{in}	650		2000	mV	PECL differential peak - peak
Data Output Voltage from GBIC to Host Board	V_{out}	370	1200	2000	mV	PECL differential peak - peak
Tx Input Impedance	Z_{in}		75		ohm	
Rx Output Impedance	Z_{out}		75		ohm	

Table 6. High-speed electrical interface - host to GBIC connector

All high-speed PECL signals to and from the copper transmission line are AC coupled internally and terminated into 75Ω (150Ω differential).

High Speed GBIC – Transmission Line Interface						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
Transmit Output Amplitude	$V_{TX, out}$	1100	1300	2000	mV	PECL differential peak - peak
Receive Input Amplitude	$V_{RX, in}$	400		2000	mV	PECL differential peak - peak
Transmitter Total Jitter at Line Output	J_t		60	112	ps	Input to GBIC from host < 192 ps jitter per IEEE802.3
Receiver Total Jitter at GBIC output	J_r		125	284	ps	Loopback through 10m cable. Input to GBIC from line < 528ps jitter per IEEE802.3
Transmit Rise/Fall Time	$T_{rise/fall}$	40		250	ps	
Tx Output Impedance	$Z_{out,TX}$		75		ohm	
Rx Input Impedance	$Z_{in,RX}$		75		ohm	

Table 7. High-speed electrical interface – GBIC to line connector

Pin Name	Pin #
+TX	1
No Connection	2
-TX	3
No Connection	4
No Connection	5
-RX	6
No Connection	7
+RX	8

Table 8. HSSDC pin assignment

V. General Specifications

General						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
Data Rate	BR		2.5, 2.125, 1.25, 1.0625		Gb/sec	Fibre Channel, IEEE 802.3 Compatible
Cable Length	L			10	m	Uncompensated cable
Bit Error Rate	BER			10^{-12}	error/sec	PRBS 2^7 - 1 test data pattern through 28m cable
Duty Cycle	--		50		%	

Table 9. General specifications

VI. Environmental Specifications

Note that the GBIC Specification requires an ambient temperature range of 0°C to 50°C. Finisar GBICs have an extended range from –10°C to +85°C case temperature as specified in Table 10.

Environment						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
Operating Temp	T_{op}	-10		85	°C	
Storage Temp	T_{sto}	-10		85	°C	

Table 10. Environmental Specifications

VII. Serial Communication Protocol

All Finisar copper GBICs are Module Definition "4", and support the 2 wire serial communication protocol outlined in the GBIC Specification[1]. Finisar GBICs use an Atmel AT24C01A 128 byte E^2PROM (with an address of 1010000X). For details on interfacing with the E^2PROM, see the Atmel data sheet titled "AT24C01A/02/04/08/16 2-Wire Serial CMOS E^2PROM."[5]

I^2C Timing Requirements						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
Atmel I^2C Clock Rate	C_{atmel}	0		100,000	Hz	Bus can be driven blind

Table 11. I^2C timing requirements

VIII. Mechanical Specifications

Finisar GBICs conform to the mechanical specifications outlined in the GBIC Specification Revision 5.4, Section 6[1].

Insertion, Extraction, and Retention Forces						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes/Conditions**
GBIC insertion	F_I	0		20	Newtons	~4.5 lbs
GBIC extraction	F_E	0		15	Newtons	~3.3 lbs
GBIC retention	F_R	130		N/A	Newtons	Straight out ~29.3 lbs

Table 12. Insertion, extraction, and retention forces

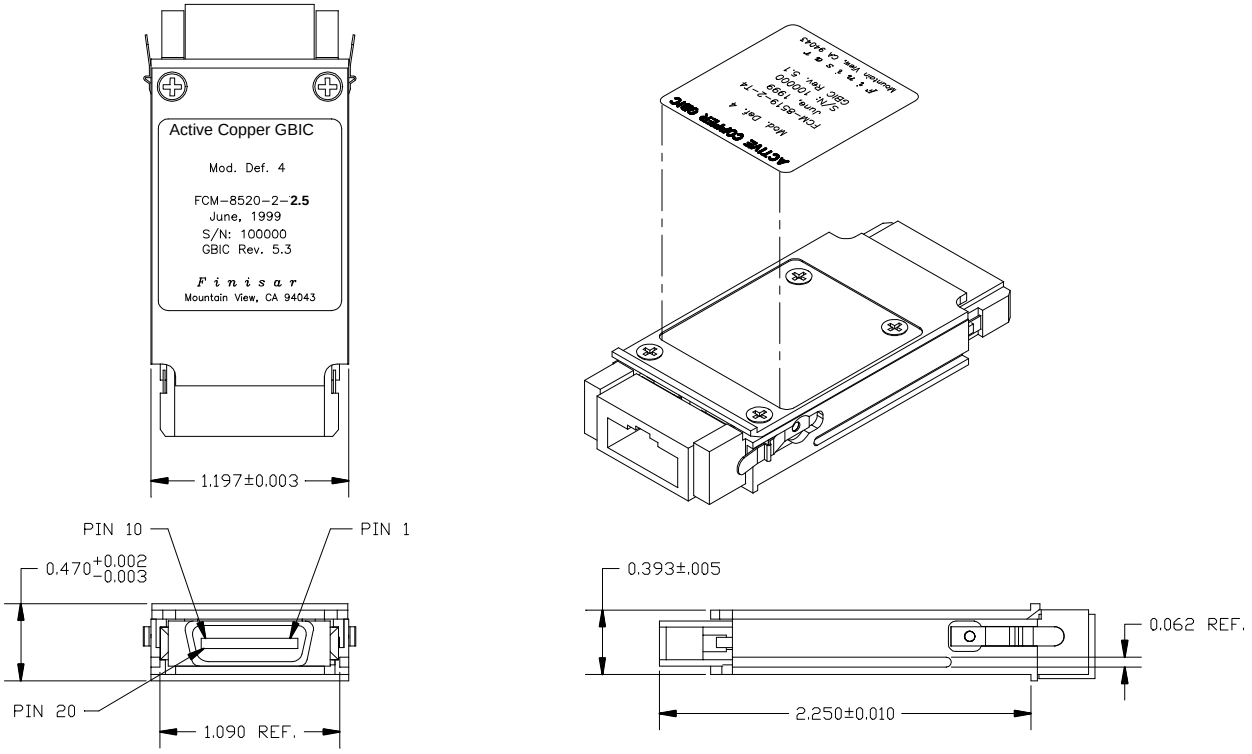

Figure 1. FCM-8520-2-2.5 Outline Drawing (HSSDC connector)

IX. References

1. "Gigabit Interface Converter (GBIC) Revision 5.4". Sun Microsystems Computer Company et. al., August 16, 1999. http://playground.sun.com/pub/OEmod/

2. "IEEE Draft P802.3z/D5.0 'Media Access Control (MAC) Parameters, Physical Layer, Repeater and Management Parameters for 1000Mb/s Operation'". IEEE Standards Department, 1998.

3. "Fibre Channel Physical and Signaling Interface (FC-PH, FC-PH2, FC-PH3)". American National Standard for Information Systems.

4. "Fibre Channel Draft Physical Interface Specification (FC-PI 7.4)". American National Standard for Information Systems.

5. "AT24C01A/02/04/08/16 2-Wire Serial CMOS E^2PROM". Atmel Corporation. www.Atmel.com

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