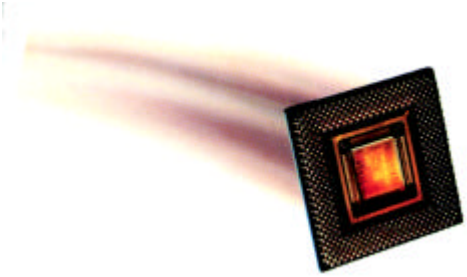
Alpha 21264 Microprocessor
Product Brief

¨ **Production June, 1998** ¨

AlphaPowered™



symbol photo

Description

The Alpha 21264 microprocessor, with benchmarks over 30 SPECint95 and 50 SPECfp95, and with spectacular bandwidths over 4 GB/s for L2 cache and over 2 GB/s for memory, enables the system designer to produce the highest performance systems ranging from PC clients to enterprise servers. The 21264 is the third-generation 64 bit Alpha Microprocessor. It includes the latest Alpha architecture enhancements, such as motion-video instructions and byte/word operations.

The 21264 completely controls its optional L2 cache and provides flexible bus timing to support a wide range of L2 cache memory devices such as those listed here:

- Commodity 133MHz register-to register burst SRAMs (2+GB/s)
- 250MHz late-write SRAMs (4+GB/s)
- 333MHz dual-data clock-forwarded SRAMs (5+GB/s)

Applications

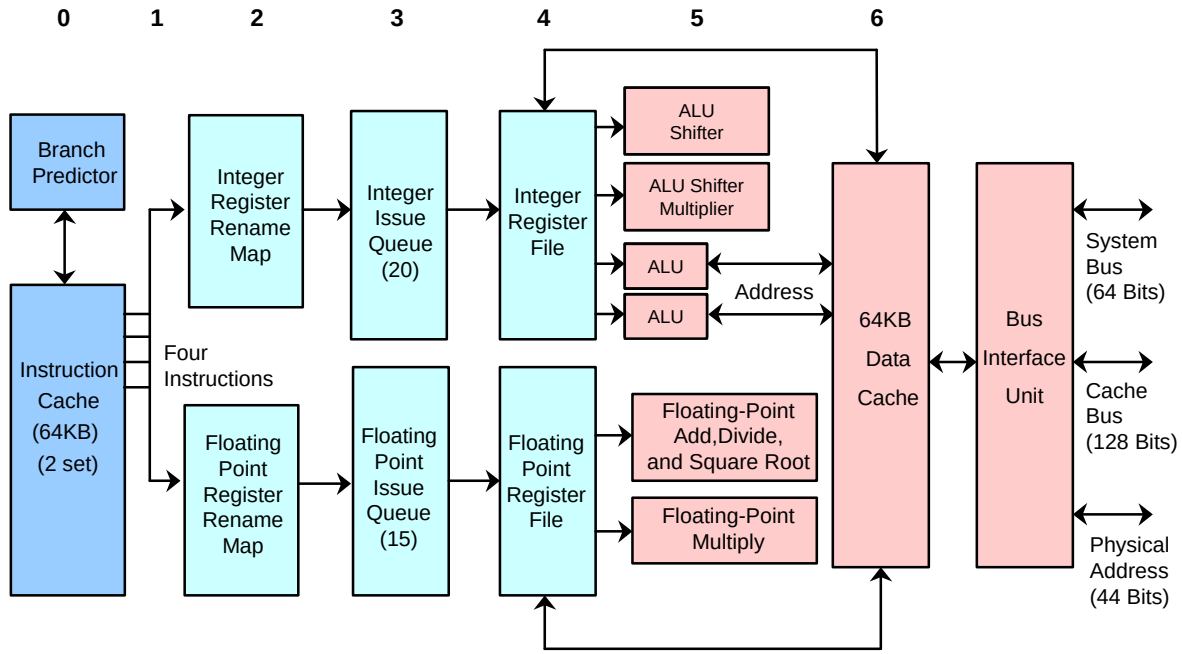
- Supports Windows NT - the world's fastest growing operating system.
  - Microsoft has chosen Alpha as the first Windows NT 64-bit platform.
  - Microsoft releases Windows NT applications concurrently for Alpha and Intel systems.
- Runs Windows 95 and non-native Windows NT applications using the Digital FX!32 binary translator.
- Supports Digital UNIX - the first 64 bit UNIX operating system.
- Supports Open VMS, V x Works, and Linux.
- Optimizes visual computing (video and 3D graphics) using its powerful floating point unit and the new Alpha motion-video instructions (MVI).
  - Real-time DVD authoring (MPEG2 and AC-3)
- Simplifies development of a single or dual Alpha 21264-based system using the 21272 core logic chipset (21272).

Benefits

- System developers can deliver a 21264 solution that:
  - Will exceed end-user expectations in performance and Windows NT compatibility.
  - Provides investment protection by way of a migration path to higher speed 21264s and future generations of Alpha microprocessor.
- The 21264 will provide end users with a quantum leap in performance that will:
  - Enable real-time visual computing.
  - Perform instant data mining .
  - Implement internet commerce.
  - Enhance medical imaging.
  - Solve the most complex, large data-set problems quickly.
  - Aid research centers in developing solutions to complex problems in disciplines such as medicine and polymers.

Pipeline Operation Sequence

The 21264 is a four-way out-of-order-issue microprocessor that performs dynamic scheduling, register renaming, and speculative execution. The 21264 pipeline contains four integer execution units. Two of the integer execution units can perform memory address calculations for load and store operations. The 21264 pipeline also contains two floating point execution units to perform add, divide, square root, and multiply functions.



The 21264 pipeline stages perform the following operations:

Cycle 0 - Instruction fetch using branch prediction
Cycle 1 - Instruction data is transferred to the register rename map hardware
Cycle 2 - Rename (map) instruction register
Cycle 3 - Issue instructions from the queues
Cycle 4 - Read register file
Cycle 5 - Execute integer or floating-point instruction
Cycle 6 - Write integer results or access cache

Characteristics	
Electrical	
Power supply	**Vss**=0.0V, **Vdd**=2.0 V ± 5%,
Operating temperature	**Tj**=100 ˚C maximum
Storage Temperature range	-55 ºC to + 125 ºC (-67 ºF to 257 ºF)
Power dissipation @ 500MHz	60W (estimated)
Package Transistor count Process Die Size	588-pin IPGA 15.2 million 0.35 micron CMOS six-layer metal Approximately 3.1.

22 January, 1998 - Preliminary -

For More Information

To learn more about the availability of the Samsung 21164 (466MHz through 600MHz) Alpha Microprocessor, contact

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