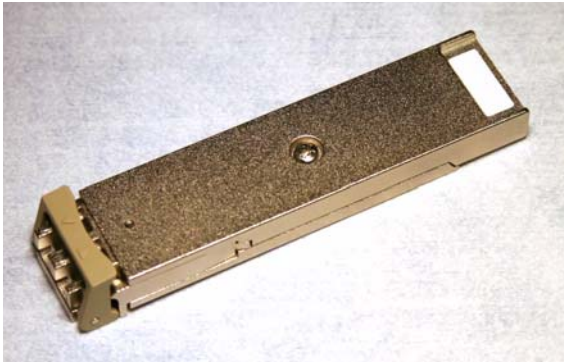


Accelar™

RoHS Compliant 10Gbps 850nm XFP Transceiver Module



PLRXXL-SC-S43-C1

Picolight's MSA compliant 10Gbps 850 nm XFP transceiver is a cost-effective, high-reliability opto-electronic (O/E) device that transmits and receives standard compliant high-speed serial 10 Gbps optical and electrical signals. The Picolight design provides a single product solution for the IEEE 802.3ae 10GBASE-SR, 10GBASE-SW, and 10GFC optical interconnects that are used in Telecommunication, Data Communication, and Storage Area Network applications. The **lead free and RoHS Compliant** transceiver features a Picolight 850 nm Vertical Cavity Surface Emitting Laser (VCSEL) and a PIN photodiode. The XFI electrical interface uses 10 Gbps differential data channels for communications to the module as specified in the 10 Gigabit Small Form Factor Pluggable Module MSA. The transceiver's MSA compliant "hot-z-pluggable" mechanical design provides the system designer a small footprint 10 Gbps solution and enables high density front-panel designs with up to 16 10G ports per line card. The PLRXXL-SC-S43-C1 is another 10Gbps product in Picolight's *Accelar* product line of 850nm transceivers targeted at short reach applications. Link lengths greater than 400m can be achieved on 2000MHz*km fiber.

Key benefits

- **Lead free and RoHS compliant**
- Industry-wide XFP MSA form factor
- Standard compliant optical specifications
- Superior thermal performance
- Dense I/O implementation
- Excellent EMI performance
- Multivendor availability
- High reliability
- Requires only 3.3V and 1.8V power supplies

Applications

- 10 Gigabit Ethernet (LAN PHY) IEEE 802.3ae 10GBASE-SR and 10GBASE-SW
- 10G Fibre Channel optical interconnects
- Cross-connect switches
- Router interconnect
- MAN aggregation links
- Computer cluster cross-connect
- Custom high-speed data pipes

<http://www.xfpmsa.org>

Highlights

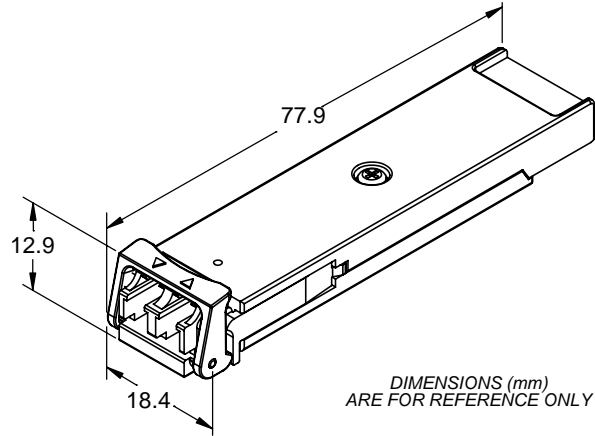
- ◆ **Lead free and RoHS Compliant**
- ◆ **Compliant to Ethernet and Fiber Channel 10 Gbps Specifications.** *Simplifies supply chain.*
- ◆ **Hot pluggable** *enables real-time in-field system upgrades*
- ◆ **Serial XFI electrical interface** *enables flexible routing for line cards and backplanes of up to 12 inches over enhanced PCB traces*
- ◆ **System monitoring and component mapping** *via I²C management interface*
- ◆ **Design based on high volume optoelectronics packaging**
- ◆ **Proven supply chain and reliable long-term supply** *based on Picolight's reliable VCSELs and PIN diodes*

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www.picolight.com

PLRXXL-SC-S43-C1 Features and Specification Highlights:

- Incorporates a directly modulated 850nm Picolight oxide VCSEL
- Low operating power consumption (<2.0W max.)
- Mechanical design features compliant with XFP MSA INF8077i Rev. 4.5
- Center-pull bail mechanism for consistent installation and removal
- 0°C To 70°C case temperature operating range
- 9.95 Gbits/s to 10.75 Gbit/s serial optical and electrical interface
- LC receptacled optical connector
- Durable plastic bail delatch mechanism
- 30 pin XFP compatible connector
- System and line-side loopback modes
- Loss of Signal (RX_LOS) Indicator
- Transmitter Disable (TX_DIS) pin
- Power Down (P_Down) pin.
- Module De-select, Module Absent, Module Reset, and Module Not Ready pins
- XFI compatible electrical interface, single differential channel operating at up to 10.75 Gbit/s
- Bit error rate < 1x10⁻¹²
- I²C interface with XFP-compliant diagnostic functions
- -5.2V, 5V, 3.3V, and 1.8V power supply compatible, only 3.3V and 1.8V required
- IEC 60825-1 Class 1 laser eye safe
- FCC Class B compliant
- ESD Class 2 per MIL-STD 883 Method 3015



PLRXXL-SC-S43-C1 Mechanical Footprint

Ordering Information

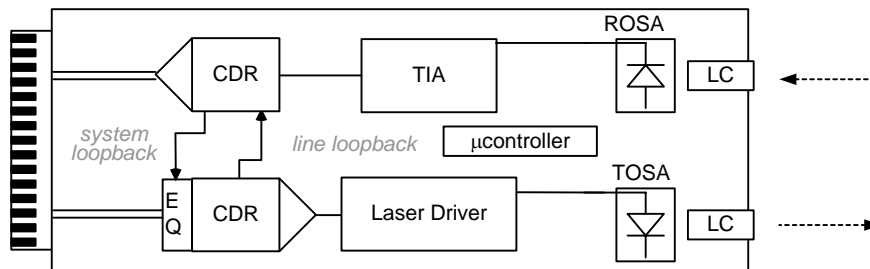
Part Number:	Description:	Contact Information:
PLRXXL-SC-S43-C1	Lead free and RoHS compliant 850nm XFP duplex LC receptacled 10 Gigabit transceiver module with beige, plastic bail	Picolight Incorporated 1480 Arthur Avenue Louisville, CO 80027 USA Tel: 303.530.3189 E-mail: sales@picolight.com Web site: www.picolight.com

Section 1 Functional description

The PLRXXL-SC-S43-C1 RoHS compliant 850 nm VCSEL-based 10 Gigabit XFP transceiver is a full duplex serial electric, serial optical device with both transmit and receive functions contained in a single module. It is designed to be compliant with IEEE 802.3ae 10GBASE-SR, 10GBASE-SW (300m), and 10 G Fibre Channel specifications. The transceiver is also fully compliant with the XFP 10 Gigabit Small Form Factor Pluggable Module Multi-Source Agreement INF8077i Rev. 4.5. This device is the ideal solution for high density, cost effective 10Gbps 850nm multimode-mode fiber (MMF) interconnects. A block diagram of the PLRXXL-SC-S43-C1 transceiver is shown in Figure 1 below.

The PLRXXL-SC-S43-C1 XFP transceiver has several low-speed interface connections including a 2-wire serial interface. These connections include; module not ready (Mod_NR), module deselect (Mod_DeSel), Interrupt, transmitter disable (TX_DIS), module absent (Mod_ABS), receive loss (RX_LOS), and power down/reset (P_Down/RST).

Figure 1 PLRXXL-SC-S43-C1 XFP transceiver block diagram



Two loopback modes are available through the two-wire serial interface. The loopback modes are useful to facilitate stand-alone testing. In system loopback mode, data recovered from the system side transmit interface is re-directed to the system side receive interface. This facilitates system side test and debug. In network loopback mode, data recovered from the line side receive interface (optics) is looped to the line side transmitter output back to the fiber.

Transmitter

The transmitter path converts 9.95, 10.3, 10.5, or 10.75 Gbps NRZ electrical data to a standard compliant optical signal. The transmitter accepts a 100 Ohm differential 120 mV peak-to-peak to 1000 mV peak-to-peak 10Gbps CML electrical signal on TD- and TD+ pins. This performance exceeds the XFI “Ziffy” specification in the XFP MSA INF8077i revision 4.5 and provides over 300 mm (12 inches) reach on improved FR4 material (loss tangent of 0.016) and offers greater flexibility to system integrators for host board layout.

Inside the module, the differential signals pass through a signal conditioner with equalization that compensates for losses and deterministic jitter present on the input data stream. A reference clock input (RefCLK+, RefCLK-) is used by the internal PLL to determine line rate and signal lock condition. The Tx clock circuit provides a lock alarm output, failure to lock results in Mod_NR asserted. The output of the Tx signal conditioner is input to the laser driver circuit which transforms the small swing digital voltage to an output modulation and bias current that drives a directly modulated 850nm VCSEL. The optical signal is engineered to meet the IEEE 802.3ae 10GBASE-SR, 10GBASE-SW, and 10 GFC specifications. Closed-loop control of the transmitted laser power over temperature and

voltage variations is provided. An LC connectorized receptacle provides the mechanical interface to the multi-mode fibre plant.

Receiver

The receiver converts incoming DC balanced serial 9.95, 10.3, 10.5, or 10.75 Gbps NRZ optical data into serial XFI electrical data. An LC connectorized receptacle provides the mechanical interface to the multi-mode fiber plant. A high speed PIN photodiode converts the optical signal into a current which is converted to a voltage in a high-gain transimpedance amplifier. The amplified signal is passed to a signal conditioning IC that provides clock and data recovery. Loss of signal, and signal lock detection is included in the receive circuitry that is reflected in the Mod_NR status pin. The recovered data is output on the RD+ and RD- pins as a 100 Ohms 250mV peak-to-peak CML signal. The output signal meets the XFP MSA requirements.

Low Speed Signaling

Low speed signaling is based on low voltage TTL (LVTTTL) operating at a nominal voltage of 3.3V

SCL/SDA: Two wire Serial interface clock and data line. Hosts should use a pull-up resistor connected to Vcc 3.3V on the two-wire interface SCL (clock), SDA (data), and all low speed outputs.

Mod_NR: Output pin. When asserted high indicates that the module has detected a condition that renders Tx and or Rx data invalid.

Mod_DeSel: Input pin. When held low by the host the module responds to 2-wire serial communication commands. When high the module does not respond to or acknowledge any 2-wire interface communication from the host.

Interrupt: Output pin. When low indicates possible module operational fault or a status critical to the host system.

TX_DIS: Input pin. When asserted high the transmitter output is turned off.

Mod_ABS: Output pin. Asserted high when the XFP module is absent and is pulled low when the XFP module is inserted.

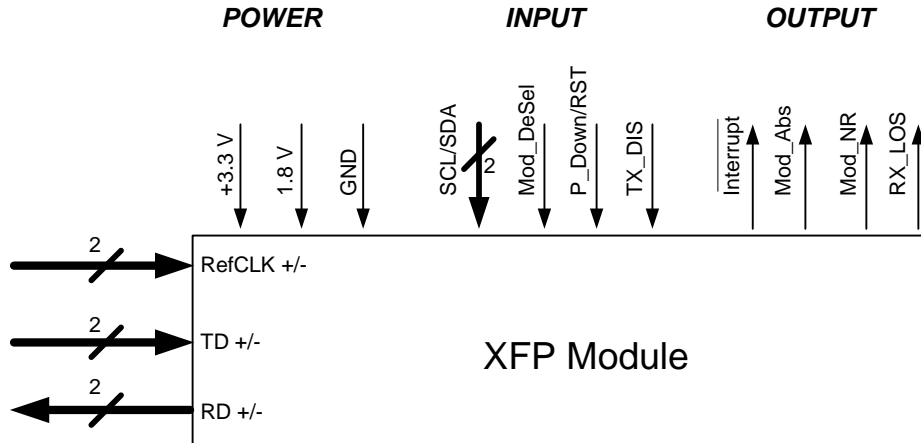
RX_LOS: Output pin. Asserted high when insufficient optical power for reliable signal reception

P_Down/RST: Multifunction input pin. The module can be powered down or reset by pulling the low-speed P-Down pin high. In power down mode no data is transmitted on the optical Tx or the electrical Rx path. The reset pulse is generated on the falling edge of the P-Down signal. Following reset, the internal PLL's must reacquire lock and will temporarily indicate a Mod_NR failure until the PLL's reacquire lock.

Section 2 Application schematics

Recommended MSA connections to the PLRXXL-SC-S43-C1 transceiver are shown in Figure 2 below.

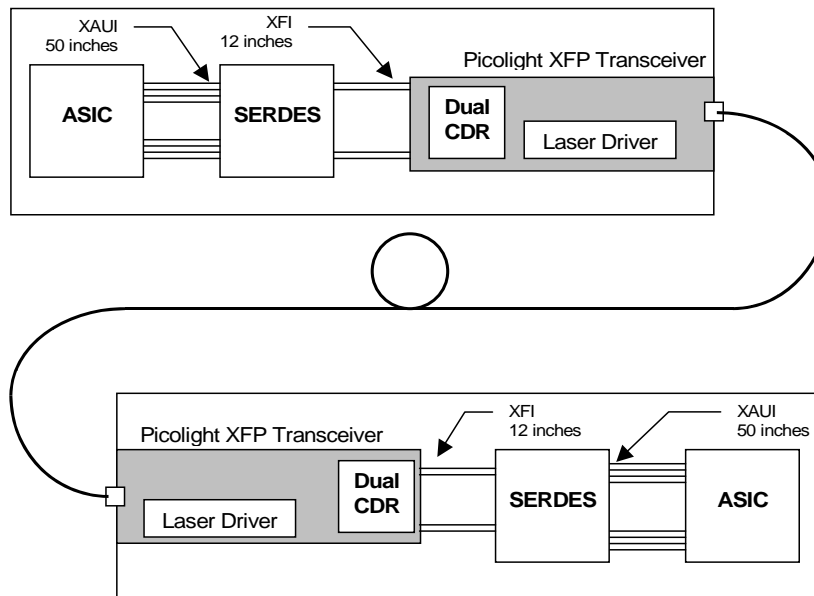
Figure 2 Application schematic for the PLRXXL-SC-S43-C1 transceiver



Power supply filtering is recommended for the PLRXXL-SC-S43-C1 module. To limit wide band noise power, the host system and module shall each meet a maximum of 2% peak-to-peak noise when measured with a 1MHz low pass filter. In addition, the host system and the module shall each meet a maximum of 3% peak-to-peak noise when measured with a filter from 1MHz-10MHz.

A typical board-to-board application using a XAUI based MAC/Framer ASIC is shown in Figure 3 below. High-speed serial 10Gbps ASICs will eliminate the need for the SER-DES IC. However, the XAUI implementation offers greater flexibility in layout as the XFI interface is limited to reaches of 12 inches (30 cm), while the XAUI interface can span over 20 inches (50 cm) on the host PCBA.

Figure 3 Board-to-board XFP application diagram



Section 3 Technical data

Technical data related to the RoHS Compliant 10Gbps 850nm XFP Transceiver Module includes:

- Section 3.1 Pin function definitions on page 6
- Section 3.2 XFP/XFI Reference model compliance points on page 8
- Section 3.3 Absolute maximum ratings on page 8
- Section 3.4 Electrical characteristics on page 8
- Section 3.5 Jitter Specifications on page 9
- Section 3.6 Input Reference Clock Specifications on page 10
- Section 3.7 Timing Requirement of Control and Status I/O on page 10
- Section 3.8 XFP 2-wire interface protocol and Management Interface on page 11
- Section 3.9 Optical characteristics on page 12
- Section 3.10 Optical link distances on page 12
- Section 3.11 Regulatory compliance on page 13
- Section 3.12 PCB layout on page 13
- Section 3.13 Module Outline on page 14
- Section 3.14 Connectors on page 14

3.1 Pin function definitions

Table 1 Transceiver pinout on host board

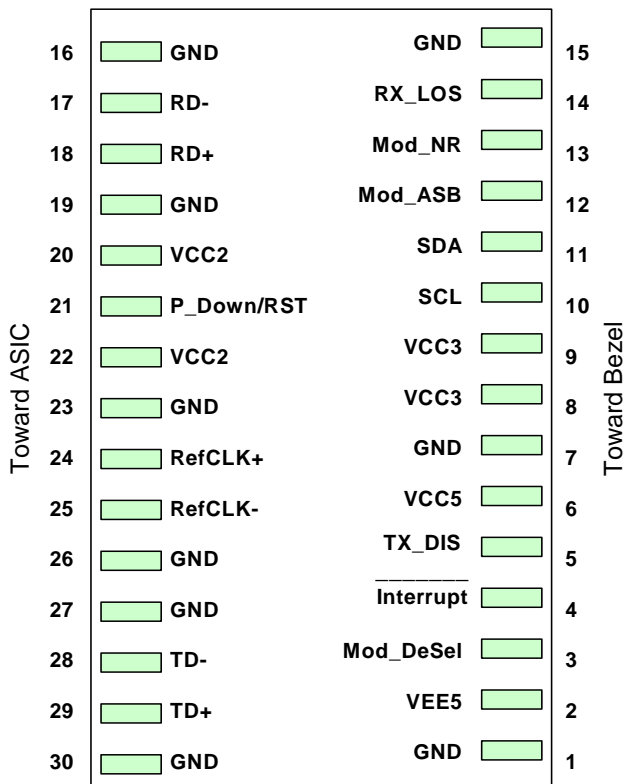
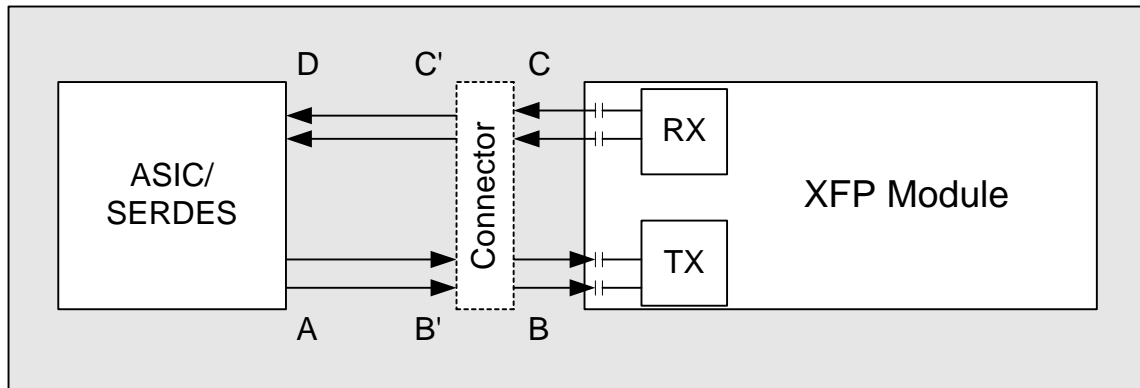


Table 2 Pin descriptions

Pin no.	Type	Name	Description
1		GND ¹	Module Ground
2		VEE5	Not Used; may be left unconnected (Optional -5.2V Power Supply)
3	LVTTTL-I	Mod_Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands”
4	LVTTTL-O	Interrupt ²	Interrupt; Indicates presence of an important condition which can be read over the serial 2-wire interface
5	LVTTTL-I	TX_DIS	Transmitter Disable; Transmitter Laser Source Turned Off
6		VCC5	+5V Power Supply (not used)
7		GND ¹	Module Ground
8		VCC3	+3.3V Power Supply
9		VCC3	+3.3V Power Supply
10	LVTTTL-I	SCL ²	Two Wire Interface Clock
11	LVTTTL-I/O	SDA ²	Two Wire Interface Data Line
12	LVTTTL-O	Mod_Abs ²	Indicates Module is not present. Grounded in the Module
13	LVTTTL-O	Mod_NR ²	Module Not Ready; Indicating Module Operational Fault
14	LVTTTL-O	RX_LOS ²	Receiver Loss Of Signal Indicator
15		GND ¹	Module Ground
16		GND ¹	Module Ground
17	CML-O	RD-	Receiver Inverted Data Output
18	CML-O	RD+	Receiver Non-Inverted Data Output
19		GND ¹	Module Ground
20		VCC2	+1.8V Power Supply.
21	LVTTTL-I	P_Down/RST	Power down; When high, the module limits power consumption to 1.5W or below. Serial interface is functional in the low power mode. Reset; The falling edge initiates a complete reset of the module including the serial interface, equivalent to a power cycle.
22		VCC2	+1.8V Power Supply
23		GND ¹	Module Ground
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board
26		GND ¹	Module Ground
27		GND ¹	Module Ground
28	CML-I	TD-	Transmitter Inverted Data Input
29	CML-I	TD+	Transmitter Non-Inverted Data Input
30		GND ¹	Module Ground

1. Module ground pins (GND) are isolated from the module case and chassis ground within the module
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board

3.2 XFP/XFI Reference model compliance points



3.3 Absolute maximum ratings

Absolute maximum ratings represent the damage threshold of the device. Damage may occur if the device is operated above the limits stated here except for brief excursions. Performance is not guaranteed and reliability is not implied for operation at any condition outside the recommended operating limits.

Parameter	Symbol	Ratings	Unit
Storage Temperature	T_{st}	-40 to +100	°C
Operating Case Temperature	T_{op}	-40 to 80 (temporary excursions)	°C
Relative Humidity	RH	5 to 95 (non-condensing)	%
Power Supply Voltages	$V_{cc2,max}$	-0.5 to 2.3	V
	$V_{cc3,max}$	-0.5 to 3.8	V

3.4 Electrical characteristics

($T_{op} = 0^{\circ}\text{C} - 70^{\circ}\text{C}$ case, unless otherwise stated)

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Supply currents and voltages						
Voltage ₃	V_{cc3}	3.13	3.3	3.47	V	With Respect to GND
Voltage ₅	V_{cc5}		5.0		V	Not used, no internal connection
Voltage ₂	V_{cc2}	1.71	1.8	1.89		VPS
Supply Current ₃	I_{cc3}		450	500	mA	
Supply Current ₅	I_{cc5}		0		mA	
Supply Current ₂	I_{cc2}		10	15	mA	VPS
Low speed control and sense signals (detailed specification in XFP MSA INF80771 Rev. 4.5)						
Outputs (Interrupt, Mod_NR, RX_LOS)	VOL	0.0		0.4	V	Rpullup pulled to host $_V_{cc}$, measured at host side of connector. IOL(max)=3mA
	VOH	host $_V_{cc}$ -0.5		host $_V_{cc}$ + 0.3	V	Rpullup pulled to host $_V_{cc}$, measured at host side of connector.

3.4 Electrical characteristics (continued)

(T _{op} = 0°C - 70°C case, unless otherwise stated)						
Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Inputs (TX_DIS, P_Down/RST, M_DSEL)	V _{IL}	-0.3		0.8	V	Pulled up in module to Vcc3
	V _{IH}	2.0		Vcc ₃ + 0.3	V	Pulled up in module to Vcc3
SCL and SDA Inputs	V _{IL}	-0.3		Vcc ₃ *0.3		Rpullup pulled to host _Vcc, measured at XFP side of connector.
	V _{IH}	Vcc ₃ *0.7		Vcc ₃ +0.5		Rpullup pulled to host _Vcc, measured at XFP side of connector.
Transmitter Input (detailed specification in XFP MSA INF8077i Rev. 4.5)						
Data Input Baud Rate Nominal		9.95	10.3125	10.75	GBd	
Data Input Bit Rate Tolerance				+/-100	ppm	
Data Input Compliance		C				internally AC coupled signals
Data Input Differential Impedance	R _I	80	100	120	Ω	
Receiver Output (detailed specification in XFP MSA INF8077i Rev. 4.5)						
Data Output Baud Rate Nominal		9.95	10.3125	10.75	GBd	
Data Output Compliance		B				internally AC coupled signals
Data Output Bit Rate Stability				+/-100	ppm	

3.5 Jitter Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Transmitter electrical input jitter from host at B (detailed specification in XFP MSA INF8077i Rev. 4.5)					
Total Non-EQJ Jitter			0.41	UI(p-p)	Total jitter less ISI
Total Jitter	TJ		0.61	UI(p-p)	
Eye Mask	X1		0.305	UI	Mask coordinate X1=0.205 if total non-DDJ is measured
Eye Mask	Y1	60		mV	
Eye mask	Y2		410	mV	50 mV is allocated for multiple reflections
Receiver electrical output jitter to host at C (detailed specification in XFP MSA INF8077i Rev. 4.5)					
Deterministic Jitter	DJ		0.18	UI(p-p)	Includes jitter transferred from the optical receiver during any valid operational input condition.
Total Jitter	TJ		0.34	UI(p-p)	
Eye Mask			0.17	UI	
Eye Mask			0.42	UI	
Eye Mask		170		mV	
Eye Mask			425	mV	
Datcom module transmitter and receiver (detailed specification in XFP MSA INF8077i Rev. 4.5)					
<i>Meets the requirements of IEEE802.3ae and 10GFC</i>					

Parameter	Symbol	Min	Max	Unit	Notes
Jitter Transfer Bandwidth	BW		8	MHz	PRBS 2 ³¹ -1, Data or scrambled 64B/66B as detailed in IEEE 802.3ae Clause 52
Jitter Peaking			1	dB	Frequency >120 KHz

3.6 Input Reference Clock Specifications

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Clock Differential Input Impedance	Zd	80	100	120	Ω	
Differential Input Clock Amplitude		640		1600	mV	AC coupled PECL
Reference Clock Duty Cycle		40		60	%	
Reference Clock Rise/Fall time	Tr/Tf	200		1250	ps	20%-80%
Reference Clock Frequency	f ₀		Baud/64		MHz	
RMS Random Jitter	σ			10	ps	up to 100 MHz
Reference Clock Frequency Tolerance	Δf	-100		+100	ppm	

3.7 Timing Requirement of Control and Status I/O

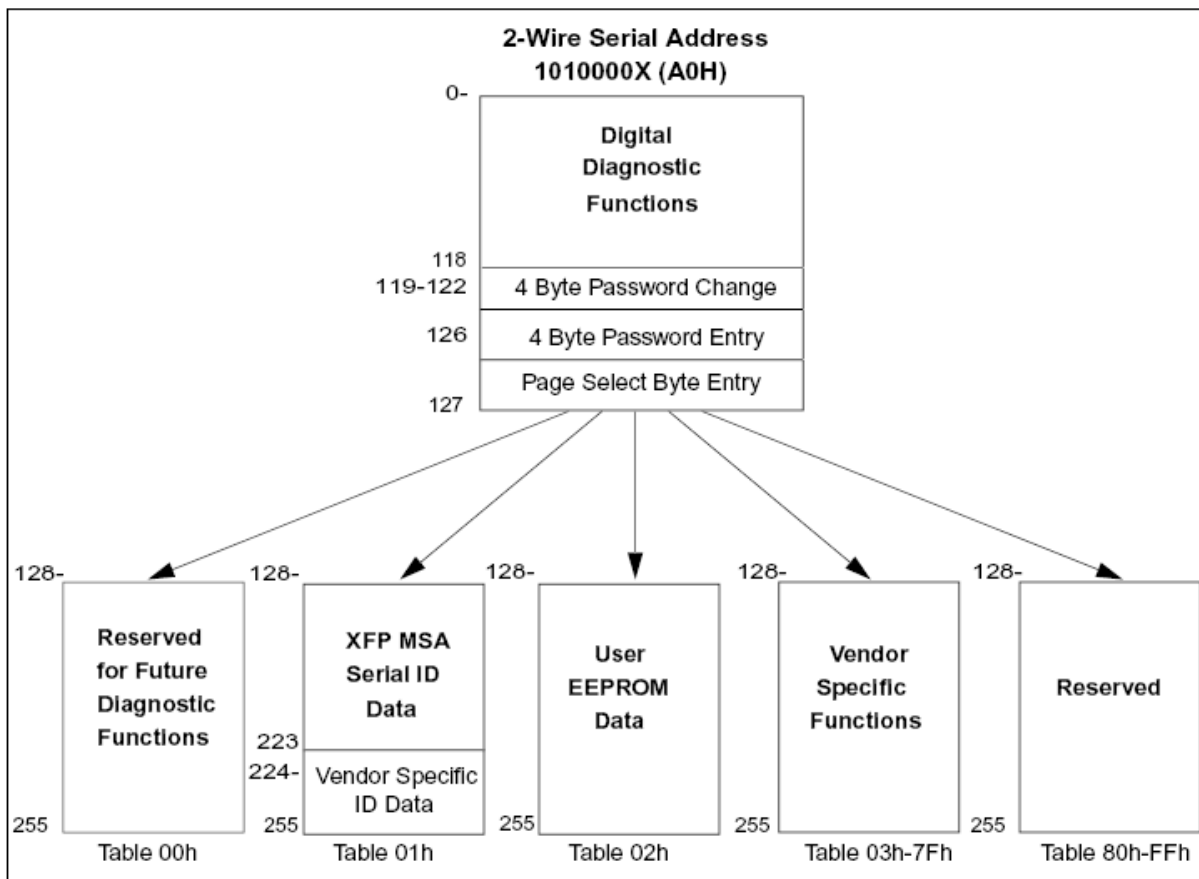
Parameter	Symbol	Min	Max	Unit	Notes
TX_DIS assert time	t _{off}		10	μsec	Rising edge of TX_DIS to fall of output signal below 10% of nominal
TX_DIS negate time	t _{on}		2	msec	Falling edge of TX_DIS to rise of output signal above 90% of nominal
Time to initialize	t _{init}		300	msec	From power on or from falling edge of P_Down/RST
Interrupt Assert Delay	Interrupt_on		200	msec	From occurrence of the condition triggering Interrupt.
Interrupt Negate Delay	Interrupt_off		500	μsec	From clear on read Interrupt flags
P_Down/RST Assert Delay	P_Down/RST_on		100	μsec	From power down initiation
Mod_NR Assert Delay	Mod_NR_on		1	msec	From occurrence of fault to assertion of Mod_NR
Mod_NR Negate Delay	Mod_NR_off		1	msec	From clearance of signal to negation of Mod_NR
P-Down Reset Time		10		μsec	Min. length of P-Down assert to initiate reset
RX_LOS Assert Delay	t _{loss_on}		100	μsec	From Occurrence of loss of signal to assertion of RX_LOS
RX_LOS Negate Delay	t _{loss_off}		100	μsec	From Occurrence of return of signal to negation of RX_LOS

2-wire serial bus timing is described in Chapter 4 of XFP MSA INF8077i Rev. 4.5

3.8 XFP 2-wire interface protocol and Management Interface

The Picolight PLRXXL-SC-S43-C1 module incorporates a XFP compliant 2-wire management interface which is used for serial ID, digital diagnostics, and certain control functions. It is modeled on the SFF-8472 Rev 9.3 specification modified to accommodate a single 2-wire interface address. In addition to the basic I2C read/write functionality the modules support packet error checking that, when enabled, allows the host system to confirm the validity of any read data. Details of the protocol and interface are explicitly described in the MSA. Please refer to the MSA for design reference.

Figure 4 XFP 2-wire serial digital diagnostic memory map



3.9 Optical characteristics

(T _{case} = 0 to 70°C)						
Parameter*	Symbol	Min	Typ.	Max	Unit	Notes
Transmitter						
Signal Speed		9.95	10.3125	10.75	Gbps	
Signal Tolerance				+/-100	ppm	
Average Optical Power	P _{Avg}	-6.5	-2.8	-1.5	dBm	
Extinction Ratio	E _r	3	6		dB	
Triple trade off curve compliance						Triple trade off curves define OMA, Spectral Width and Center Wavelength (any two parameters fix the third)
OMA (Optical modulation amplitude)	OMA	380	600	1200	uW	
RMS Spectral Width	Δλ		0.25	0.45	nm	
Center Wavelength	λ _p	840	850	860	nm	
Relative Intensity Noise	RIN _{12OMA}			-128	dB/Hz	
Transmitter and Dispersion Penalty	TDP			3.9	dB	
Return Loss Tolerance				12	dB	
Receiver						
Signal Speed		9.95	10.3125	10.75	GBd	
Wavelength	λ _p	840		860	nm	
Return Reflectance				-12	dB	
Average Receive Power				-1.0	dBm	
Stressed Rx Sensitivity OMA	S _S			-7.5	dBm	
Bit Error Ratio	BER			10 ⁻¹²		Without FEC
* See IEEE 802.3 Clause 52 Media Access Control (MAC)Parameters, Physical Layer, and Management Parameters for 10 Gb/s Operation for complete specification						

3.10 Optical link distances

Data Rate	Fiber Type	Modal Bandwidth @ 850nm (MHz-km)	Worst Case Distance Range Specified (m)	Typical Range (m)
9.95-10.3125 Gbps	62.5/125um MMF	160	2 - 26	
	62.5/125um MMF	200	2 - 33	
	50/125um MMF	400	2 - 66	
	50/125um MMF	500	2 - 82	
	50/125um MMF	2000	2 - 300	>400

3.11 Regulatory compliance

The PLRXXL-SC-S43-C1 is lead-free and RoHS-compliant per Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

The PLRXXL-SC-S43-C1 complies with international Electromagnetic Compatibility (EMC) and international safety requirements and standards (see details in Table 3 on page 13). EMC performance is dependent on the overall system design. Information included herein is intended as a figure of merit for designers to use as a basis for design decisions.

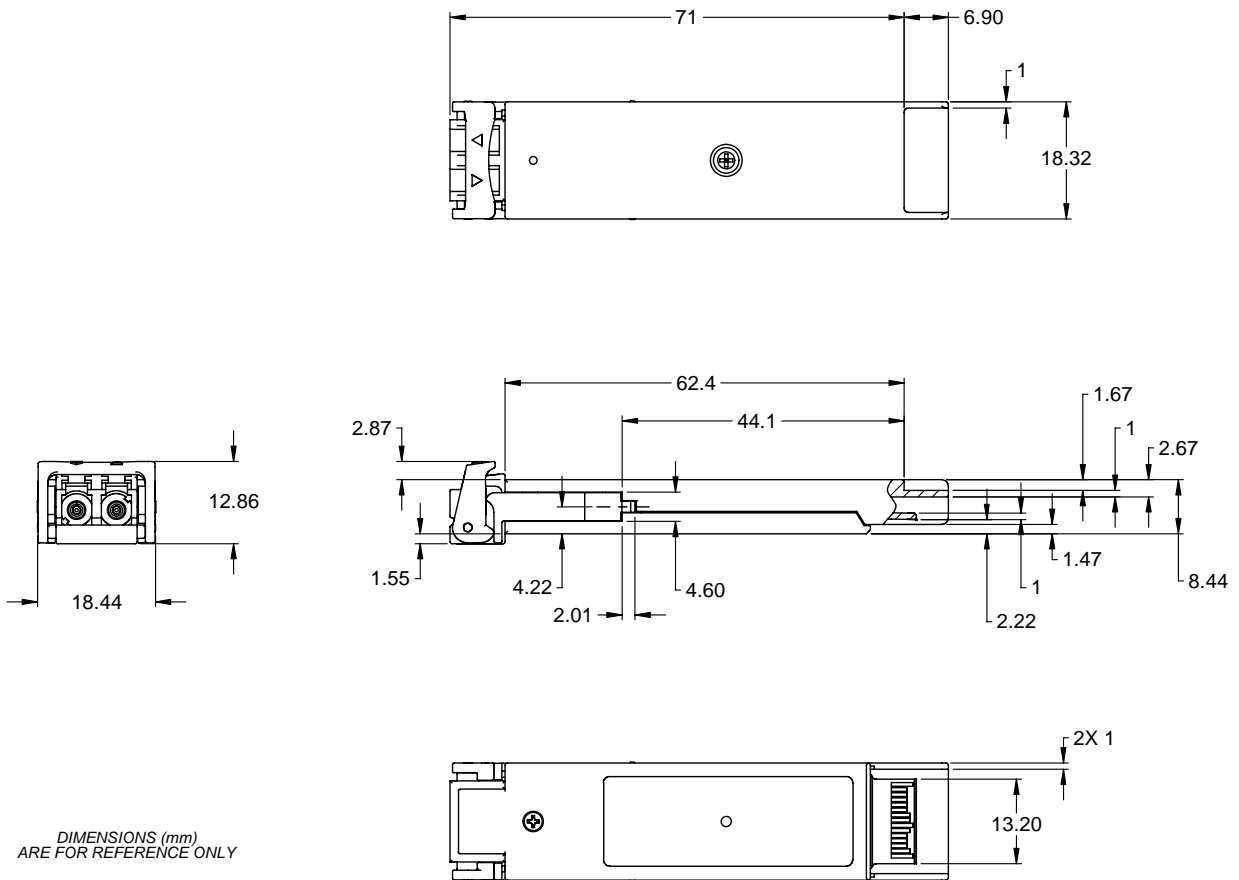
Table 3 Regulatory compliance

Feature	Test Method	Performance
Component Safety	UL 60950 UL94-V0 EN 60950	UL File E209897 TUV Report/Certificate (CB Scheme)
RoHS Compliance	Directive 2002/95/EC	Compliant per the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
Laser Eye Safety	EN 60825 U. S. 21CFR 1040.10	TUV Certificate CDRH compliant and Class 1 laser eye safe
Electromagnetic Compatibility		
CE	EU Declaration of Conformity	Compliant with European EMC and Safety Standards
Electromagnetic Emissions	EMC Directive 89/336/EEC FCC CFR47 Part 15 IEC/CISPR 22 AS/NZS CISPR22 EN 55022 ICES-003, Issue 4 VCCI-03	Noise frequency range: 30 MHz to 40 GHz. Good system EMI design practice required to achieve Class B margins.
Electromagnetic Immunity	EMC Directive 89/336/EEC IEC /CISPR/24 EN 55024	
ESD Immunity	EN 61000-4-2	Exceeds Requirements. Withstands discharges of; 15kV contact, 25kV air
Radiated Immunity	EN 61000-4-3	Exceeds Requirements. Field strength of 10V/m RMS, from 10 MHz to 1 GHz. No effect on transmitter/receiver performance is detectable between these limits.

3.12 PCB layout

Recommended PCB layout is given in XFP MSA INF8077i Rev. 4.5

3.13 Module Outline



3.14 Connectors

Fiber

The XFP module has a duplex LC receptacle connector.

Electrical

The electrical connector is the 30-way, two row PCB edge connector. Customer connector is Tyco/AMP Part No. 788862C or equivalent.

Section 4 Related information

Other information related to the RoHS Compliant 10Gbps 850nm XFP Transceiver Module includes:

- Section 4.1 Package and handling instructions below
- Section 4.2 ESD discharge (ESD) below
- Section 4.3 Eye safety on page 16

4.1 Package and handling instructions

Connector covers

The PLRXXL-SC-S43-C1 is supplied with an LC duplex receptacle. The connector plug supplied protects the connector during standard manufacturing processes and handling by preventing contamination from dust, aqueous solutions, body oils, or airborne particles.

Note: It is recommended that the connector plug remain on whenever the transceiver optical fiber connector is not inserted.

Recommended cleaning and de-greasing chemicals

Picolight recommends the use of methyl, isopropyl and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (e.g. trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrrolidone).

This product is not designed for aqueous wash.

Housing

The PLRXXL-SC-S43-C1 housing is made from zinc.

4.2 ESD discharge (ESD)

Handling

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and operation

In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transceiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

Typical of optical transceivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization at the higher layers (e.g. Serializer/Deserializer chip).

4.3 Eye safety

The PLRXXL-SC-S43-C1 is an international Class 1 laser product per IEC 60825-1 Amendment 2 (2001) and IEC 60825-2 1997. The PLRXXL-SC-S43-C1 is an eye safe device when operated within the limits of this specification.

Operating this product in a manner inconsistent with intended usage and specification may result in hazardous radiation exposure.

CAUTION!

Tampering with this laser based product or operating this product outside the limits of this specification may be considered an act of "manufacturing," and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (21 CFR 1040).

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