| | | |
|---|---|---|
| d i g i t a l | Level of Urgency | Page 1 Of 15 |
| FCO | [ R ] | |

FIELD CHANGE ORDER — Number DEQNA-R001

Applicability: Any Micro-PDP11 or Micro-VAX LSI-Bus systems which are attached to Ethernet using the DEQNA at revision level "D" or earlier will need the "Required" FCO. Replace all M7504 (DEQNA) modules below Rev "E1/E2" with reworked devices. Purge all units from the shelf stock in the Field Logistics Stockrooms and SR# 17 which have not been ECO'ed (M7504-MK005) and return for rework to rev "E1/E2." This FCO implements ECO M7504-MK005.

Problem/Symptoms: Undetected Data Corruptions can occur and/or a device "lock-up" can be seen when the DEQNA is busy with a transmit pre-fill operation and a receive message comes in. The DEQNA will appear to be hung and requires a device or system reset to clear the "lock-up."

Quick Check: Presence of chip # 23-087K4-00 in location E11.

| Compatibility/Prerequisite FCO: | Est. Time to Install |
|---|---|
| None | 1.0 Hours |

Special Tools or Test Equipment:
None

FCO Parts Information

| Order by FCO Kit # | Contents | | |
|---|---|---|---|
| | Quantity | Part Number | Description |
| EQ-01418-01 | 1 | M7504 ("E1/E2") | DEQNA module Rev "E1/E2" |
| FA-04703-01 | 1 | | DEQNA FCO documentation |

EQ Kit Variation/System-Option Applic: Micro-PDP11's & Micro-VAX's

Approvals

| CSSE Engineer | F.S. Product Safety | F.S. Logistics |
|---|---|---|
| Dave Waterman | William Henry | Ed Duggan |
| **Responsible CSSE Mgr** | **F.S. Microfiche Libraries** | **Affected Population** |
| Tony Payne | EP-FSNVX-LB VAX | 30,000 |

| ESD&P Micropublishing | EP-FSP11-LB PDP-11 | Initial Kitting |
|---|---|---|
| Terry Page | | 30,000 |
| | VAXnotes | |
| Revision | STARS | Hardcopy Publication |
| A | | 30,000 |
| FCO Release Date | | Parts Availability |
| 04-June-1986 | | June 1986 |



!! ATTENTION !!

TO THE INSTALLER OF THIS DEQNA M7504 MODULE:

PLEASE READ THIS FIRST!

REWORK PROCEDURES FOLLOW ON PAGE 10 OF THIS FCO.

PLEASE BE SURE TO PASS THIS DOCUMENTATION PACKAGE TO THE SYSTEM MANAGER OF THE SYSTEM INTO WHICH THIS DEQNA M7504 MODULE (REVISION E1 OR HIGHER) IS INSTALLED.

THANK YOU.

Dear DEQNA User:

Digital’s number one priority is commitment to quality and customer satisfaction. Due to this commitment, we have been strenuously testing the DEQNA and have discovered some problems that are now corrected by this upgraded M7504 module. Software aid recovery processes for the specific DEQNA problems have already been applied to the major Digital operating systems; however, the complete solution is in the form of this upgraded DEQNA module, plus the software changes.

Digital has minimized the impact to customers by making these changes transparent. Digital assures that the changes to the DEQNA allow for continued operation with Digital standard drivers. In addition, this DEQNA module has been shipped with documentation that identifies the changes so customers having non-Digital custom drivers can make modifications, if necessary. The customer is responsible for modifying such custom drivers and for the operation of custom drivers, based on the documentation provided with this DEQNA module.

Included with this documentation package is a series of descriptive notes:

1. HOW TO IDENTIFY THE REV. E1 OR HIGHER M7504 DEQNA MODULE

2. SOFTWARE CHANGE RECOMMENDATIONS FOR CUSTOM DEQNA DEVICE DRIVERS

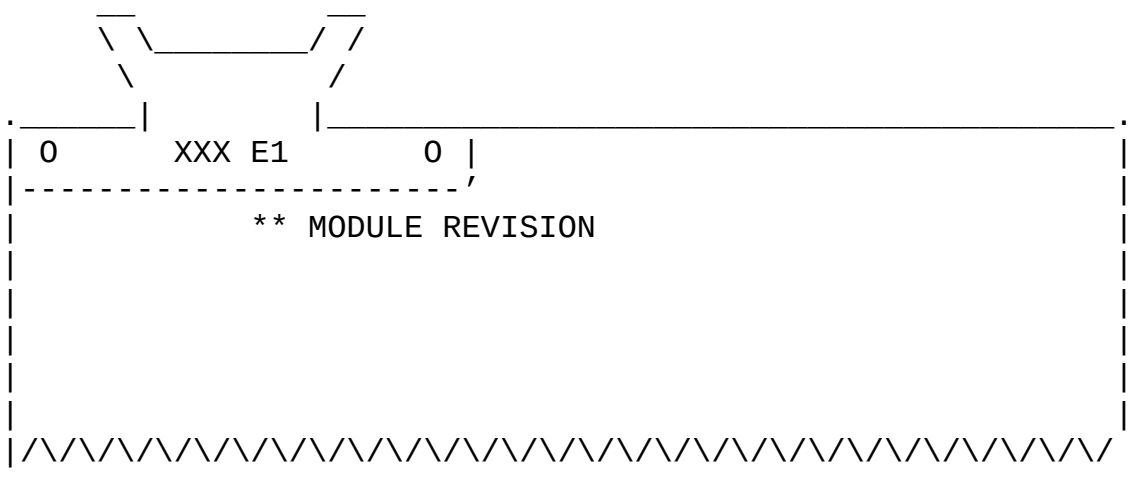
3. DIGITAL SOFTWARE VERSIONS WHICH HAVE/ WILL HAVE RECOMMENDED CHANGES IMPLEMENTED

For more information regarding this DEQNA upgrade, please contact your local Field Service Office and/or Sales Representative.

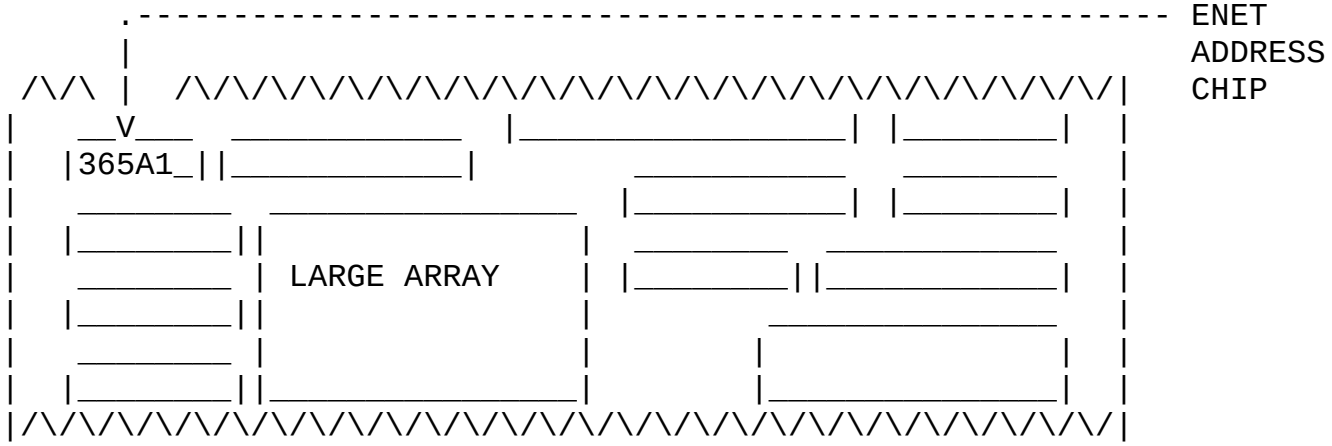
HOW TO IDENTIFY A REV. E1 OR HIGHER M7504 DEQNA MODULE

THIS PICTORIAL IS DESIGNED TO AID IN EASY DETECTION OF A REV. E1 OR HIGHER DEQNA UPGRADED MODULE (M7504). THE MODULE REVISION IS STAMPED ON THE BOTTOM OF THE PLASTIC HANDLE VISIBLE ON SIDE TWO (BOTTOM SIDE) AS REFERENCED BELOW. ADDITIONALLY, IF YOUR APPLICATION SOFTWARE IS DEPENDENT UPON THE DEQNA M7504 PHYSICAL ETHERNET ADDRESS, IT MAY BE NECESSARY TO EXCHANGE THE CHIP ON THE "OLD" MODULE WITH THE CHIP ON THE "NEW" MODULE. THE SOCKETED CHIP IS LABELED AS "ENET ADDRS" (365A1) AS IDENTIFIED IN THE SECOND PICTORIAL.

PICTORIAL REPRESENTATIONS
OF MODIFIED DEQNA
- M7504 -




SIDE 2 (BOTTOM)




SIDE 1 (TOP)

# SOFTWARE CHANGE RECOMMENDATIONS FOR DEQNA CUSTOM DEVICE DRIVERS

IMPORTANT:

THE TOTAL SOLUTION FOR THE DEQNA PRODUCT PROBLEMS IS A HARDWARE FCO AND THE IMPLEMENTATION OF THESE SOFTWARE CHANGES.

IT IS RECOGNIZED THAT BOTH THE SOFTWARE CHANGES AND THE HARDWARE FCO WILL NOT BE INSTALLED SIMULTANEOUSLY; THIS POSES NO PROBLEM. THE NEW MODULE WILL WORK WITH THE UNCHANGED SOFTWARE, AND THE CHANGED SOFTWARE WILL WORK WITH THE PRE-ECO HARDWARE. IN BOTH CASES, NO NEW PROBLEMS ARE INTRODUCED.

Some of this information may currently exist in the DEQNA User's Guide, but the importance of this data will be stressed in the descriptions that follow. Digital assumes no responsibility for custom drivers for the DEQNA, but is supplying this information to assist those customers who have such a device driver by providing accurate and timely information regarding DEQNA operation.

## 1. RECEIVE BUFFERS

### 1.1 NUMBER OF RECEIVE BUFFERS

Software should be configured to contain a large number of Receive buffers (at least 20 on a network with heavy traffic.)

Failure to allocate a sufficient number of Receive buffers may cause the DEQNA to pause while waiting for more buffers in which to empty the FIFO. This pause will inhibit any transmit from completing, because the transmit status information is relayed through the FIFO serially with the receive data.

### 1.2 SIZE OF RECEIVE BUFFERS

Receive buffers may be any size; however, the SUM of the Receive buffers' sizes should exceed 1600 decimal bytes. The DEQNA will continue placing packet data into the next buffer if the current buffer is not large enough to hold a complete packet. Some events on the Ethernet may cause the DEQNA to

process more than the maximum legal size Ethernet message. To be safe, Receive buffers' sizes should be a minimum of at least 1600 decimal bytes.



SOFTWARE CHANGE RECOMMENDATIONS FOR DEQNA CUSTOM DEVICE DRIVERS (continued)

Failure to reserve 1600 bytes for the Receive buffers will cause the DEQNA to seemingly "hang". But, the condition is really that the DEQNA is waiting for buffer space to store the incoming packet and is not actually "hung".

### 1.3 RECEIVE BUFFERS *MUST* START ON A WORD-ALIGNED BOUNDARY.

Do not assign a Receive buffer starting address at an odd-byte address boundary.

Assignment of Receive buffer odd-byte address boundaries may cause the DEQNA to "miss" reception of the first byte; thus, odd-byte address boundaries must be avoided.

## 2. TRANSMIT BUFFERS

### 2.1 TRANSMIT BUFFER ADDRESS

Transmit buffers MUST begin on a word-aligned boundary.

FAILURE to start Transmit buffers on a word-aligned boundary can cause an EXTRA byte within the transmit packet. This extra byte gets calculated into the hardware CRC; thus, the error will not be detected.

### 2.2 SIZE OF TRANSMIT PACKETS

The sum of the bytes contained in the one or more buffers that comprise one complete transmit packet must not exceed 1518 bytes.

The DEQNA will accept over 1518 bytes; however, after 1518 bytes are reached, the set-up table within the DEQNA will be overwritten. As a result, the DEQNA may not respond to

set-up addresses that were previously defined.

## 3. BUFFER DESCRIPTOR LISTS

### 3.1 SETTING UP BDL

Before setting the BDL Address Descriptor Bit to indicate a VALID entry, ALL other information in the buffer descriptor must be valid. The VALID bit must be the LAST bit (or entire word) written.



### 3.2 CHAINING

The last entry on the chain list must be a buffer descriptor that has the Address Descriptor bit (bit 15) clear, indicating an empty entry. This applies equally for Transmit and Receive lists.

FAILURE to leave an empty entry could cause the DEQNA to reuse buffers on the list.

### 3.3 LIST MODE

There must be two words left clear at the end of the Receive and Transmit buffer descriptor lists.

FAILURE to do this will result in having the two words following the last buffer descriptor being overwritten.

### 3.4 RECEIVE BDL STATUS WORD 2

Make both bytes of Status Word 2 unequal when setting up the Receive BDL. When the DEQNA has finished the receive operation associated with a BDL, it will make both bytes of Status Word 2 equal. Status Word 2 information is not to be considered valid data from the DEQNA until both bytes are equal.

### 3.5 MULTIPLE BUFFERS FOR ONE RECEIVE MESSAGE PACKET

When the DEQNA uses more than one Receive buffer to store an incoming packet, Status Word 1 bits 15 and 14 are the only valid bits of the buffer descriptor pointing to the interim buffer. All other bits in the Status Word 1 buffer descriptor are reserved and should not be sampled. The Status Words contained in the buffer descriptor of the last buffer used to store the packet may be sampled to gather information about that packet.

## 4. SET-UP PACKETS

Normal set-up packets should be less than 128 decimal bytes in length. If there is a need to use a set-up packet that is greater than 127 decimal bytes, then Receive Enable (in the DEQNA's CSR) must be negated before queuing the set-up packet. Reassert Receive Enable when the set-up packet completes.



## 5. TRANSMIT SERVICE ROUTINE

### 5.1 BEFORE EXITING

The routine that queues a Transmit Buffer Descriptor list must check the status of DEQNA CSR bit 5 (Receive List Invalid) to make sure that it is not set. If the Receive List Invalid bit is set, then the DEQNA must be given new Receive buffers.

FAILURE to maintain a valid Receive list may cause a failure to interrupt on completion of a transmit. If DEQNA CSR bit 5 is set, then a transmit complete interrupt will not occur.

### 5.2 TRANSMIT TIMER

The device driver must have a minimum 1-2 second timer on the Transmit Interrupt to allow software to recover from a transmit "hang" on the DEQNA.

Most operating systems (VMS, RSX, ULTRIX) will have a timer (because of DECNET considerations) in the higher levels of software, thus negating the need for this kind of timer in the driver. There are no "hang" conditions in the new Rev. E1 or higher M7504 DEQNA module.

## 6. RECEIVE SERVICE ROUTINE

### 6.1 BEFORE DEFERRING SERVICE

On Receive interrupt, determine which of the buffers do contain packets that are to be discarded, e.g., Runt Packets, and return the availability of those buffers to the DEQNA. This will allow the DEQNA to have maximum Receive buffers available for use. Other servicing of the Receive packet can occur at a non-interrupt service level.

### 6.2 BEFORE EXITING

Make sure that all Receive buffers are processed and that the Receive List Invalid bit (DEQNA CSR bit 5) is clear prior to exiting the service routine.



### 6.3 TIMEOUT COUNTER

A timeout counter should be set for 15 seconds. If no message has been received within 15 seconds, then the DEQNA CSR bit 5 should be checked. If bit 5 is set, process the Receive buffers.

## 7. BROADBAND

See the DECOM User’s Manual for programming practices regarding the DECOM transceiver. Transmit Buffer Descriptor Status Word 1 LOSS bit (bit 12) should be ignored on all transmits.

DIGITAL SOFTWARE PACKAGE VERSIONS WHICH HAVE/
WILL HAVE THE RECOMMENDED CHANGES IMPLEMENTED

| SOFTWARE | VERSION |
|---|---|
| MicroVMS | V4.4 |
| Ultrix-32M | V1.2 |
| Ultrix-11 | V3.0 |
| VAXELN | V2.1 |
| RT-11 | V5.3 |
| MicroPower/Pascal | V2.1 |
| DECnet-Micro/RSX | V4.2B |
| DECnet-11M, M | V4.2B |
| DECnet-11M, M-Plus | V3.0B |
| DECnet-11S, S | V4.2B |



## REWORK PROCEDURE

1. Power down the LSI-Bus system (Micro-PDP11 or Micro-VAX) which houses this M7504 module by setting the console key switch or circuit breaker to the "off" position.

```
**************************************************************
*                        CAUTION                             *
*       TO ASSURE THAT THE AC POWER IS REMOVED FROM THE      *
*       UNIT, THE CIRCUIT BREAKER LOCATED IN THE REAR OF     *
*       UNIT MUST BE SET TO THE "OFF" (0) POSITION, OR       *
*       THE AC POWER CORD MUST BE DISCONNECTED.              *
**************************************************************
```

2. Remove the M7504 module to be upgraded from the LSI-Bus system.

3. Check to see if the M7504 is at Rev "E1/E2" or higher by verifying that the quick check chip (P/N 23-087K4-00) is present in location E11 (see diagram below in step 5).

4. If the module does not have the quick check hardware installed as mentioned in step 3 above, then install the M7504 module from the EQ-01418-01 Kit material supplied herein.

5. Assure that all applicable jumpers and switches on the new M7504 are configured in the same manner as the module being removed. BE SURE TO EXCHANGE THE ADDRESS ROM IN LOCATION E42 (THE 16 PIN DIP, AS SHOWN ON THE NEXT PAGE) FROM THE OLD MODULE TO THE NEW MODULE TO GUARANTEE THE DEQNA ADDRESS REMAINS THE SAME (this will assure that software being down-line-loaded is still addressing the correct node address).

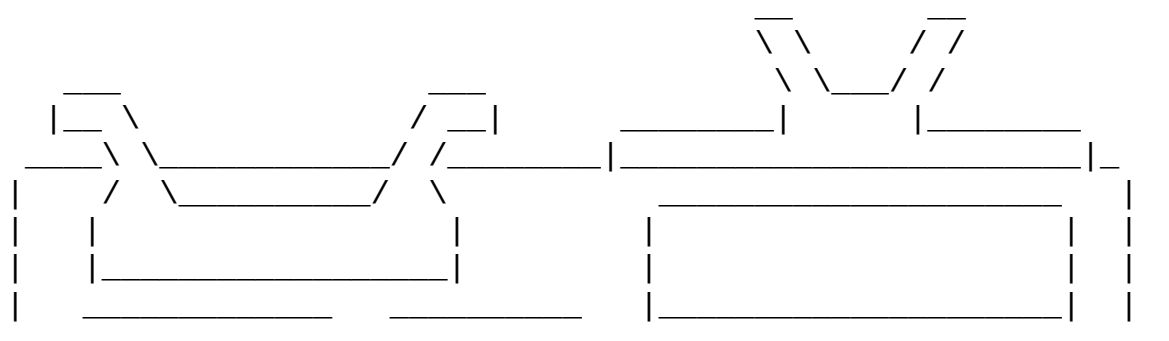


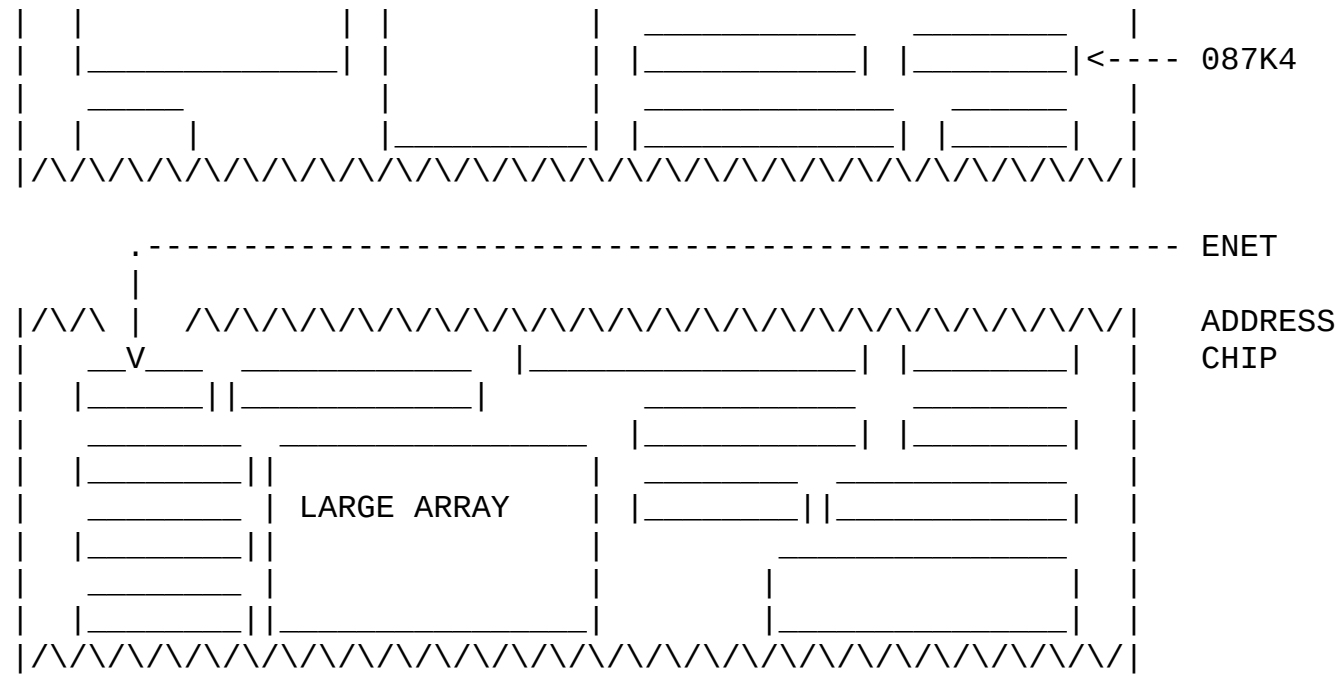
## REWORK PROCEDURE

### HOW TO IDENTIFY A REV E1 OR E2 M7504 DEQNA MODULE

THIS PICTORIAL IS DESIGNED TO AID IN EASY DETECTION OF A REV E1 OR E2 DEQNA REWORKED MODULE (M7504). THE IDENTIFYING FEATURE WHICH WILL ALLOW EASY DETECTION OF THE E1 OR E2 M7504 MODULE IS THE 087K4 LABELED COMPONENT IN THE UPPER RIGHT HAND CORNER OF THE MODULE AS SHOWN BELOW. ADDITIONALLY, IF YOUR APPLICATION SOFTWARE IS DEPENDENT ON THE DEQNA M7504 PHYSICAL ETHERNET ADDRESS, IT MAY BE NECESSARY TO EXCHANGE THE CHIP ON THE "OLD" MODULE WITH THE CHIP ON THE "NEW" MODULE. THE CHIP IS CLEARLY LABELED AS "ENET ADDRS" AND IS IDENTIFIED IN THE SECOND PICTORIAL.

PICTORIAL REPRESENTATION
OF MODIFIED DEQNA
- M7504 -








## REWORK PROCEDURE

6. Install the FCO’ed module into the LSI-Bus slot where the old module was removed.

7. Package the old M7504 up using the packing material provided for by the EQ Kit module. USING THE PROPER FS LOGISTIC SUPPLIED RED TAG, TAG THE M7504 AND MARK IT APPROPRIATELY AS NEEDING REWORK ONLY OR REPAIR AND REWORK! Assure that this module gets returned expeditiously to the returns area upon completion of this call to ensure future allocations can be issued. Return this unit with an SBA containing the following information:

    a. Revision level for the M7504 modules being returned.
    b. Serial numbers for the M7504 modules being returned.
    c. Reason for the return - FCO upgrade, repair and/or DOA.

8. Power-up the LSI-Bus system and run system and device diagnostics to verify goodness of the new hardware.

9. Request the customer load, run, and verify the operating system software

to accept the system back after the FCO upgrade. Assure the customer is aware of the recommended software workaround recommendations supplied in this EQ Kit as both the software and this FCO hardware are required to guarantee all problems have been resolved.

10. Fill out LARS report as per the attached examples (pages 13 through 15).

\^ DEQNA
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