Avago Technologies Evaluation Board Kit for Small Form-Factor Pluggable Transceivers with Digital Monitoring Interface (SFP w/DMI)

Application Note 1300

SFP Evaluation Board

The purpose of this Digital Small Form Factor Pluggable (SFP) evaluation board kit is to provide the designer with a convenient means for evaluating Avago Technologies GbE and Fibre Channel SFP w/DMI transceivers, as well as future SFP w/DMI MSA compatible product offerings.

This document describes the details of the evaluation printed circuit board (PCB) and the test equipment and methods for evaluating the optical/electrical characteristics of SFP modules. In addition, hardware and software for evaluating the digital interface of SFP w/DMI modules are recommended. The detailed operation of the SFP w/DMI modules and test equipment used with this evaluation PCB kit are not described in this document, but can be found by obtaining the appropriate documents from the reference section.

Document Outline

I. Equipment List

II. Evaluation PCB Description

III. Electro-Optical Test Configuration(s)

IV. Digital Interface Test Configuration

V. Overview of Contents of Digital Diagnostic EEPROM pages

VI. Evaluation PCB Schematic

VII. Evaluation PCB Bill of Materials

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I. Equipment List

Included:

1. Evaluation PCB
2. SFP transceiver module(s)

Not Included:

1. 3.3 V dc power supply
2. Fiber optic cables
   - LC to SC (1 M and 50/125 µm or 62.5/125 µm)
   - LC to LC Loopback (<1 M and 50/125 µm or 62.5/125 µm)
3. 86100A Agilent Digital Communications Analyzer (DCA)
4. Agilent Optical/Electrical DCA Plug-In Module 86101A Option H41 or H21 (2125 FC)
5. 86130A Agilent BitAlyzer 3 Gb/s Bit Error Rate Tester (BERT)
   - Pattern generator, error detector/analyzer
6. Fiber Optic Attenuator (optional)
7. EEPROM reader software (optional)
8. PC (optional)
9. PC to two-wire serial interface adapter (optional)

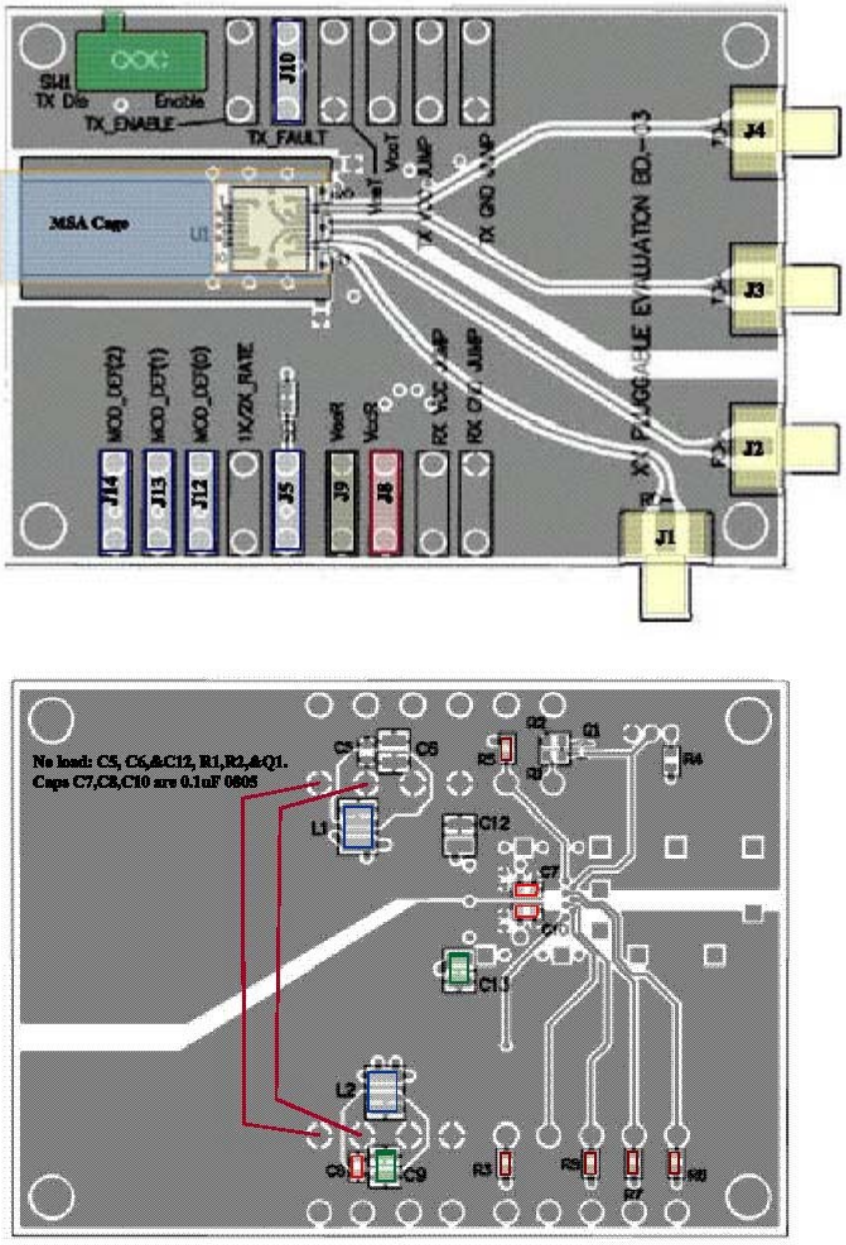

Figure 1. SFP Evaluation Board Top and Bottom View

Table 1: I/O Description

Reference Designator	Name	Description	Signal Level
J1	RD -	Differential receiver outputs	Note 1
J2	RD +		
J3	TD +	Differential transmitter inputs (< 2.4 V)	Note 1
J4	TD -		
J5	SD(LOS)	Signal Detect (LOS) Output: Low indicates sufficient optical power, High indicates insufficient optical power	LVTTL*
J6	VccT	Transmitter Power, no part: jumped to J8	3.3 V
J7	VeeT	Transmitter Ground	GND
J7	VeeT	Transmitter Ground, no part: jumped to J9	GND
J8	VccR	Receiver Power	3.3 V
J9	VeeR	Receiver Ground	GND
J10	TX Fault	Transmitter Fault Output: High output indicates a laser fault, Low indicates normal laser operation	LVTTL*
J12	MOD_DEF (0)	Module Definition 0- grounded by module to indicate that the module is present	LVTTL*
J13	MOD_DEF (1)	Module Definition 1, interfaces to EEPROM. Clock line of serial interface	LVTTL*
J14	MOD_DEF (2)	Module Definition 2, interfaces to EEPROM. Data line of serial interface	LVTTL*
J15	TX VCC JUMP	No Connect, Jump between left and right sides of board implemented with wire on underside.	
J16	TX GND JUMP		
J17	RX VCC JUMP		
J18	RX GND JUMP		
J19	TX_ENABLE	Not Connected, Can be used to electrically to switch TX_DISABLE	
SW1	TX_DISABLE Switch	Transmitter Disable Input: Enable (low signal) enables the transmitter, Disable position (high signal) disables the transmitter.	LVTTL*
U1	SFP Cage Pad	Module plugs here	
	1X/2X Rate	Rate Select Pin, Not Connected	

Notes

1. See specific transceiver data sheet for recommended maximums and further information

* LVTTL defines a 3.3 voltage level with transitions at 0.8 and 2.0 V.

II. Evaluation PCB Description

Top and bottom views of the evaluation PCB are shown in Figure 1. A description of all of the Input/Output (I/O) interfaces on the PCB is shown in Table 1, all of which are found, on the topside of the PCB. The evaluation PCB is a 4-layer design compatible with high-speed signal I/O rates required by 2.125 Gbd Fibre Channel.

III. Electro-Optical Test Configuration(s)

The two basic test configurations for evaluating the SFPs are shown in Figure 2 (Transmitter) and Figure 3 (Receiver or Loopback). These test configurations use one evaluation board the test instruments from the equipment list such as a Bit-Error-Ratio Tester (BERT) and a Digital Communication Analyzer (DCA). General considerations from the test configuration follow, but more specific details on SFP transceiver testing can be found in the documents listed in the reference section of this document.

Transmitter Configuration:

This configuration is shown in Figure 2. The SFP's optical characteristics can be tested including the eye diagram, jitter, and rise/fall time. A representative eye diagram for an SFP is shown in Figure 4. In this configuration, the receiver is not used, however it is recommended that RD- and RD+ be terminated by 50 ohm matched loads. It is also recommended that low loss, low dispersion, and equal length RF cables be used to connect TD+/- to the test equipment.

Receiver Configuration:

This configuration is shown in Figure 3. The SFP's electrical characteristics can be tested including the receiver electrical eye diagram, jitter, and rise/fall time. A representative eye diagram for an SFP is shown in Figure 5.

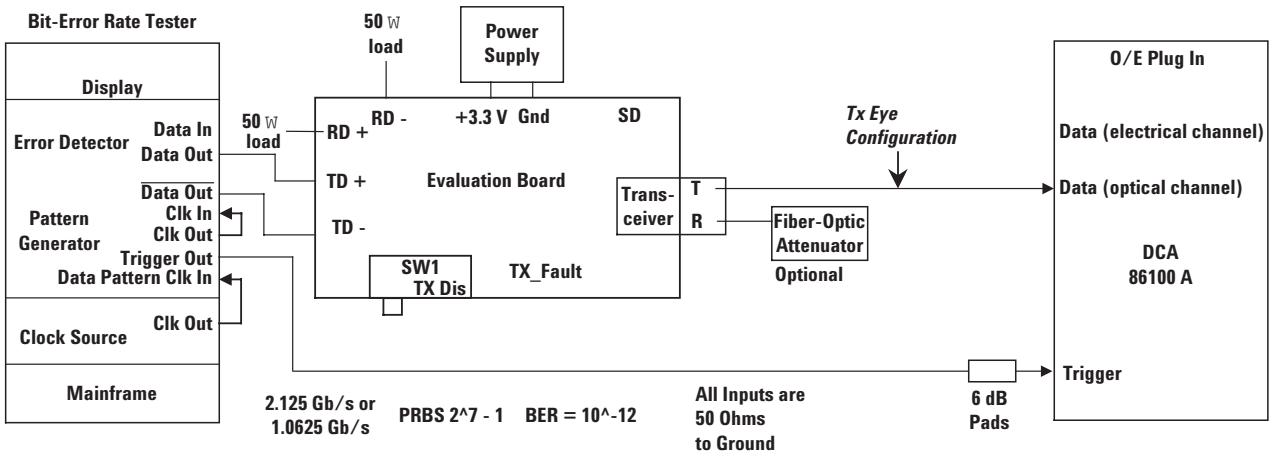

Figure 2. Recommended Transmitter Test Configuration

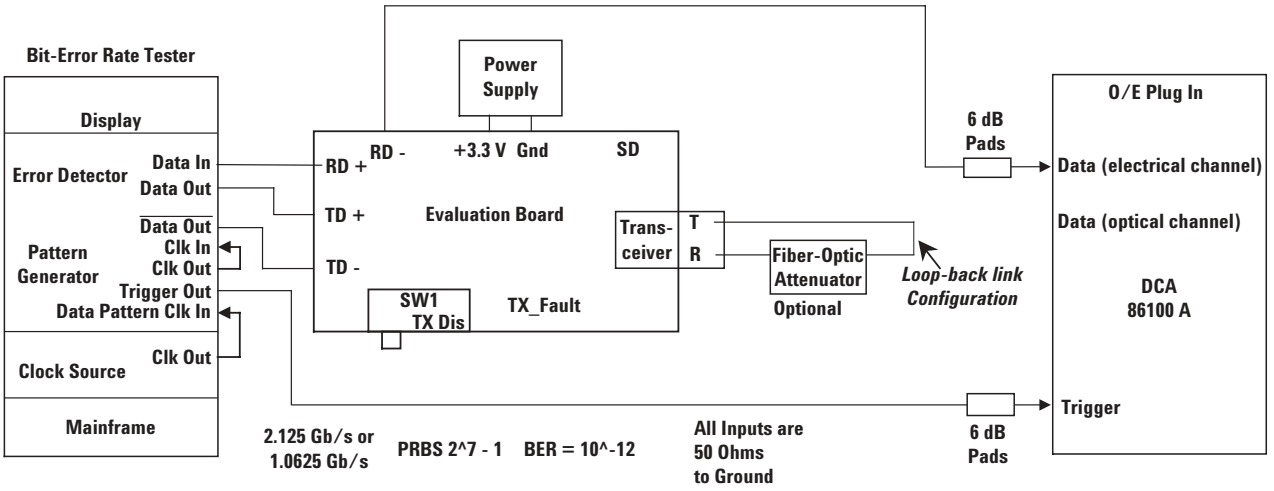

Figure 3. Recommended Receiver Configuration

Results

The following example measurements were made using the configurations illustrated in Figures 2 and 3 respectively.

IV. Digital Interface Test Configuration

The SFF-8472 MSA defines an enhanced digital interface which is a superset of the MOD_DEF two wire serial interface defined in the SFP MSA. The two wire serial interface protocol can be used to allow the user to read the contents of the two digital SFP EEPROM pages. The EEPROM page device address are A0 and A2 in hexadecimal format as defined in the SFF-8472 MSA. This is done via MOD_DEF(1) and MOD_DEF(2) connections on the evaluation board. Note that the MOD_DEF(0) is grounded by the module to indicate that the module is present an is not used during read operation.

A recommended test configuration for reading the Digital SFP EEPROM pages is illustrated in figure 6. As shown in the figure, a PC to two-wire serial hardware adapter is used to allow the user to communicate with the digital SFP module via a PC. Using custom PC software, a user can then read specific bytes from the EEPROM pages. The following optional software/adapter bundles can be implemented to read and write to SFF-8472 compatible devices:

1) Win-I2CNTDLL – a complete 32-bit PC based I^2C software/adapter bundle. The Windows-based software allows straightforward reading of the EEPROM page contents.
2) iPort (by MCC) – Windows to I^2C Bus Host Adapter. When purchased, it includes iPort Utility Pack Software for Windows[2].

Notes:

1. Details on the use of the above hardware/software reader bundles for two wire serial interface evaluation are described in their respective user manuals.
2. Additional EEPROM reader freeware software (customized for use with the Avago Technologies SFP w/DMI modules) for use in conjunction with the iPort serial interface adapter, can be made available to customers and users. Please contact your local Avago Technologies sales representative.

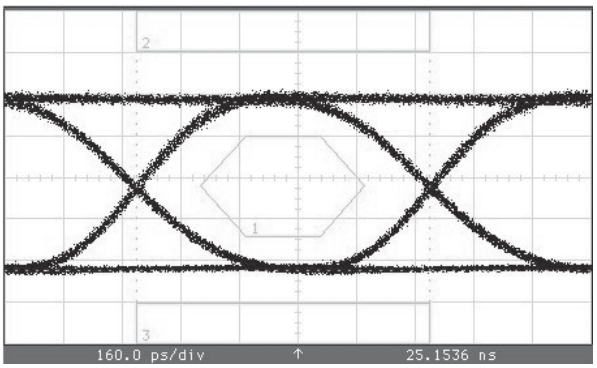

Figure 4. Example Transmitter Eye Diagram

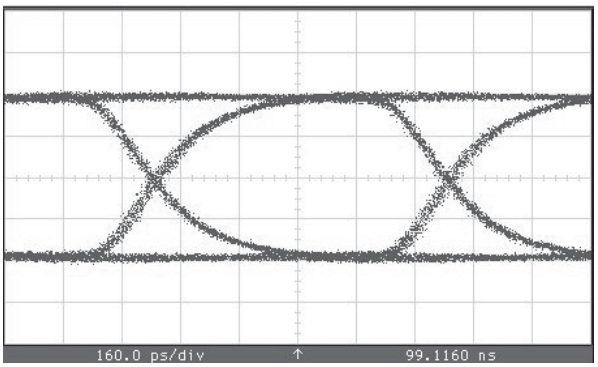

Figure 5. Example Loop Back Receiver Eye Diagram-17dBm power

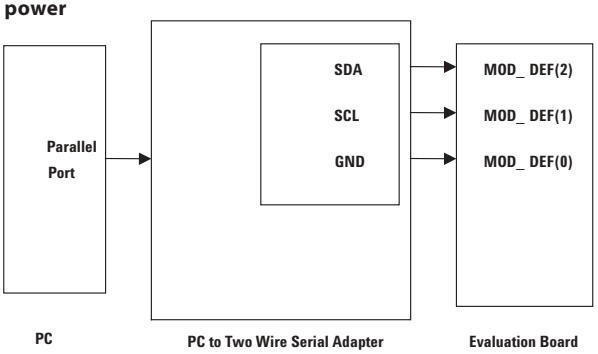

Figure 6: Recommended Digital Interface Test Configuration

V. Overview of Contents of Digital Diagnostic EEPROM Pages

The present section very briefly summarizes the byte contents of a digital SFP's EEPROM pages (addresses A0h and A2h per SFF-8472 MSA.) For more detailed information, please refer to the SFF-8472 MSA document, or the respective product data-sheets.

As noted in the SFF-8472 MSA, the digital diagnostic interface is an extension of the interface defined in the SFP MSA. Both documents specify a 256-byte memory map located in address 1010000X (A0h), accessible over a two wire serial interface. The A0h page contains serial ID information for the specific module in question (defined by SFP MSA), as well as some vendor specific data.

In addition to the A0h page defined in the SFP MSA, the digital diagnostic MSA defines a 256-byte memory map located in address 1010001X (A2h), for storing diagnostic information about the module's current operating conditions. Figure 7 illustrates the memory map for the two EEPROM pages as well as data field descriptions.

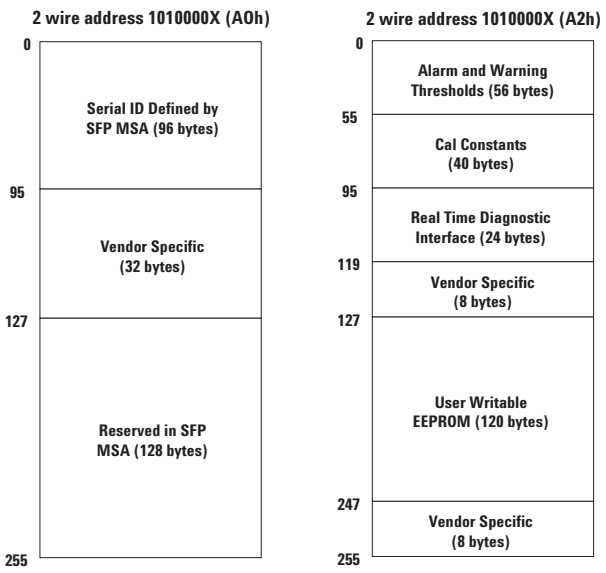

Figure 7. Digital diagnostic memory map - specific data field descriptions (from SFF-8472 MSA).

Diagnostic read-backs

Via the two wire serial interface, the user can access internal measurements of the transceiver temperature, supply voltage, transmitter bias current, transmitter output power, and received optical power. That information is stored on bytes 96 through 105 of address A2h in the following format (per SFF-8472 MSA):

1) Internally measured transceiver temperature – Represented as a 16 bit signed two's complement value, in increments of 1/256 degrees Celsius. Byte 96 is temp MSB (most significant byte), byte 97 is temp LSB (least significant byte.)
2) Internally measured transceiver supply voltage (Vcc) – Represented as a 16 bit unsigned integer with the voltage defined as the full 16 bit value (0 to 65535) with least significant bit equal to 100 μV. Byte 98 is Vcc MSB, Byte 99 is Vcc LSB.
3) Measured TX bias current in μA – Represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0 to 65535) with least significant bit equal to 2 μA. Byte 100 is the TX bias MSB, byte 101 is TX bias LSB.
4) Measured TX output power in mW – Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 to 65535) with least significant bit equal to 0.1 μW. Byte 102 is TX power MSB, Byte 103 is TX power LSB.
5) Measured RX received optical power in mW – Value can represent either average rceived power or OMA depending how bit 3 of byte 92 (A0h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 to 65535) with the least significant bit equal to 0.1 μW. Byte 104 is RX power MSB, Byte 105 is RX power LSB.

VI. Evaluation Board Schematic

The SFP evaluation board electrical schematic is shown in Figure 8 at the end of this document. The user may notice connections on the board which are not represented on this schematic (Figure 8) or pin description (Table 1). This is due to optional functionality of the board. For simplicity and ease of application, only those connections and parts included are described in schematic and bill of materials (Table 2).

VII. Evaluation PCB Bill of Materials

Table 2 below lists the evaluation board components, including brief component descriptions, comments and relevant values.

VIII. References

1. HFBR-57xx Product Data Sheets **http://www. avagotech.com**
2. Avago Technologies Application Notes (AN) **http://www. avagotech.com**
3. Small Form Factor Pluggable (SFP) Multisource Agreement **http://www. avagotech.com/ morpheus/docs/final_public_sfp_msa. pdf**
4. Digital Diagnostic Monitoring Interface for Optical Transceivers (SFF-8472) Multisource Agreement. **http://www.SFFCOMMITEE.COM**
5. Test Equipment User Manuals **http://www. avagotech.com**
6. ATMEL 2-Wire Serial Interface for AT24C01A/02/04/ 08/16 Family. **http://www.atmel.com**

Table 2: SFP Evaluation Board Bill of Materials.

Component	Type	Value	Footprint	Comments
PCB	SFP Evaluation Board			Unpopulated 4 layer circuit board
U1	Surface Mount socket (20 pin)			AMP 1367073-1
	Case jacks			0 (4 off), Advance Interconnect part 1718 or Cambion 450-3704-01-03-00
Q1	Transistor		UMX3N	Rohm dial npn transistor, not included
	Device jacks			
	Nose jacks			0 (2 off), Cambion part 450-3704-01-03-00
R3, R5, R6, R7, R8	Resistor	4.7 K	805	
C5, C7, C8, C10	Capacitor	0.1 µF	805	10% Tolerance
C6, C9	Capacitor	10 µF	Case code B	Tantalum 20% Tolerance
C13	Capacitor	10 µF	Case code B	Tantalum 20% Tolerance
L1, L2	Inductor	1 µF	1812	
SW1	Switch			Apem 25336NA
J1, J2, J3, J4	End launch SMA jack- tab contact			Johnson Components part number 142-0701-851
J5	Jack, 2 mm white			SD, Signal Detect
J8	Jack, 2 mm red			VccR
J9	Jack, 2 mm black			VeeR, RX_GND
J10	Jack, 2 mm white			TX_FAULT
J12, J13, J14	Jack, 2 mm white			MOD_DEF

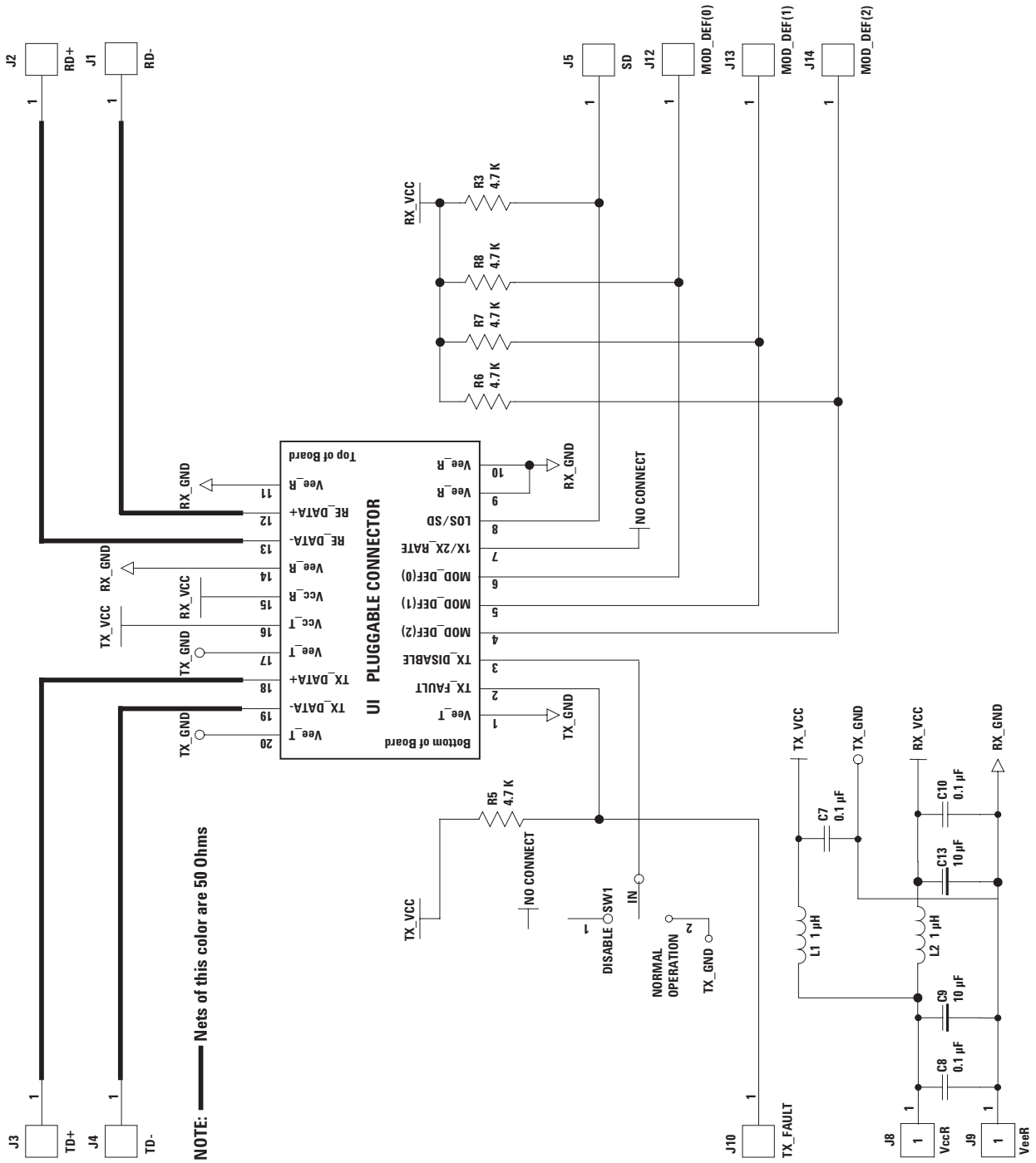

Figure 8. SFP Evaluation Board Circuit

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