



For Transmission Quality Analysis of IP Network Transmission Devices and Modules

D3371

- Frequency range : 10 Mbps to 3.6 Gbps
- Wide range of amplitude with excellent output waveform quality.
- Capable for gigabit Ethernet, SONET/SDH. etc.
- Jitter test function for ITUT-T recommendation G958, etc.
- Waveform quality measurement (eye aperture/eye diagrams/ Q values.)



D3371

3.6 G Transmission Analyzer

Overview

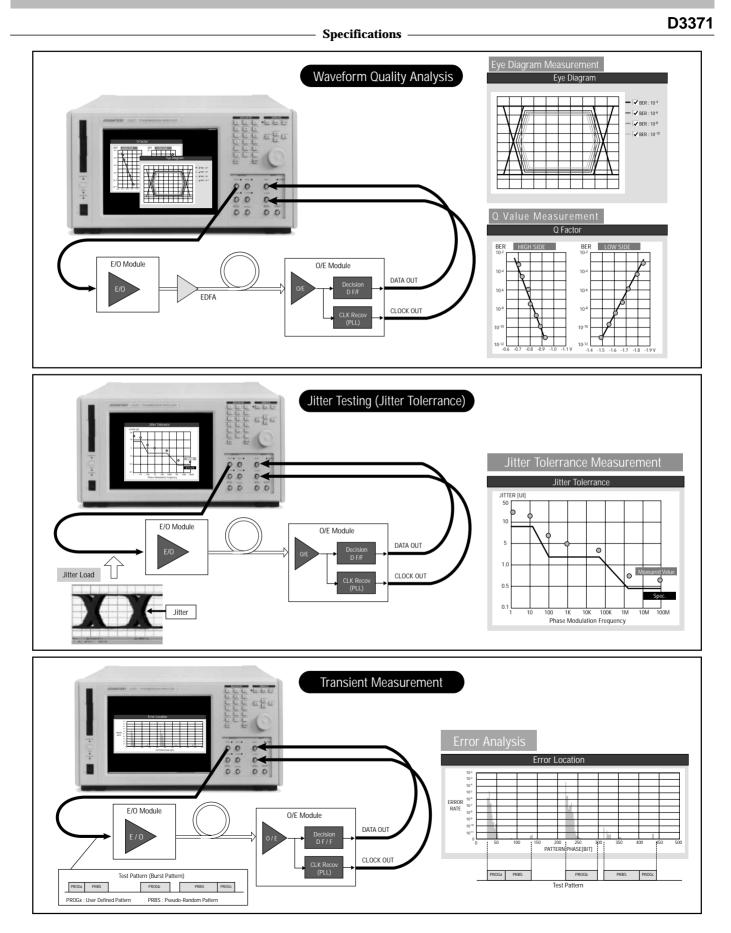
The D3371 combines a PPG (pattern generator) for generating test patterns and an ERD (bit error detector) for measuring bit errors and other phenomena in the device under test into a single compact unit.

The D3371 is equipped with a powerful range of functions that meet the requirements of the IP Network market, including Gigabit Ethernet and SONET/SDH, supporting a full range of interfaces with optical modules and devices, and with an extensive range of test patterns for simulating real line traffic, waveform quality measurement, jitter test, and bit error analysis functions. This makes the D3371 the answer to a wide range of needs from development to production and maintenance.

Features

- Capable of generating various test patterns with a wide range of amplitudes, used for applications such as EA modulation LD, low amplitude devices, etc. providing output pattern waveforms of outstanding quality.
- Capable of generating various test patterns for gigabit Ethernet, SONET/SDH. etc.
- Built-in jitter test (jitter equivalent) function for ITUT-T recommendation G958, etc.
- High performance waveform quality measurement with eye aperture/eye diagrams/Q values
- Error location analysis function allowing analysis of transient response with burst data and other phenomena.
- Supports a wide range of interfaces including ECL and PECL.
- Combines PPG, ERD, and synthesizers in single unit.
- Large color touch-panel LCD and Windows-based user interface.

For Transmission Quality Analysis of IP Network Transmission Devices and Modules



New 12.5Gbps Pulse Pattern Generator for SDH/SONET

D3186

- Excellent output waveform quality
- Generation of SDH/SONET frame patterns (mixed patterns) which is similar to actual data
- 8 M-bit memory, PRBS 31.
- Multi-channel output : 2 data channels, 3 clock channels, and 7 sub-rate channels
- Cross point variable for output waveform
- Burst signal output
- 3 Vp-p outputs, effective for EA modulators, etc. (option)



D3186 Pulse Pattern Generator

To accommodate transmission of large-capacity information in the coming multimedia generation, ultra high-speed digital telecommunications networks are being constructed.

For evaluation and analysis of O/E and E/O modules and ultra high-speed logic devices used for multiplexers and repeaters for telecommunications systems, a signal source with high speed and high quality is necessary.

The D3186 Pulse Pattern Generator/D3286 Error Detector offers excellent waveforms with high speed and high quality and diverse error detecting functions in an operating frequency range from 150 Mbps to 12.5 Gbps.

In addition, with the 8 M-bit large capacity memory and ADVANTEST's frame pattern generation function, the D3186/D3286 is a new generation of error performance test

system which is compatible with STM-1 (155.52 Mbps) to STM-64 (9.95 Gbps) in SDH/SONET.

■ Offers Excellent Waveform Quality

- For Performance Evaluation of Optical Components High quality for waveform is essential to evaluate the performance of laser diodes and optical components for optical telecommunication. To meet this demand, the D3186 Pulse Pattern Generator provides excellent waveforms with high speed and high quality. In addition, the D3186 has a wide cross point variable range for the output waveform that makes it easy to control the output waveform correction mark ratio.
- Use As a Modulation Signal Source for Optical Modulators When use with the Q7606A/B Lightwave Modulation Test Set from ADVANTEST, the D3186 provides a suitable modulation signal source in a chirp measurement system for optical modulators.
- Excellent Waveform Quality
 Through output waveform re-timing, a data output waveform with
 excellent eye balance, low jitter, and low distortion has been realized.

- Generation of SDH/SONET Frame Patterns Close to Actual Data
- For Evaluation of Optical Transmission Equipment and E/O and O/E Modules

In O/E and E/O tests of the SDH/SONET system etc, testing at the frame level is required. In addition to the large WORD memory with 8 M-bit length, the D3186 Pulse Pattern Generator is provided with an optional function to insert WORD patterns in the header section of the STM frame and arbitrary PRBS in the payload section, realizing test patterns which are very close to actual data. Of course, the D3286 error detector can measure errors at the header and payload sections separately. In addition, the D3286 powerfully supports location of cause of errors by means of the frame synchronization function and specific area error measurement function.

■ Applicable to Fiber Loop Testing

In long-distance transmission testing, fiber loop-based transmission evaluation is performed. In this test, bit error measurement for irregular burst condition data is essential. The D3186 pulse pattern generator can output a burst signal based on an external gate signal and the D3286 enables bit error measurement for burst condition data. This allows the fiber loop transmission test to be performed efficiently.

New 12.5Gbps Pulse Pattern Generator for SDH/SONET

D3186

■ Equipped with 8-Mbit Memory and 31-Stage PRBS

The D3186 generates up to six STM-64 frames (in the WORD pattern mode and mixed SDH pattern mode). With ATM transmission, noncontinuous data are transmitted and therefore the function to generate as long memory patterns as possible is required in evaluation using memory patterns.

Multi-Channel Output Consisting of 2 Data Output, 3 Clock Output and 7 Sub-Rate Output

In evaluation of transmission system and devices, different data and clock signals and frequency rate are required according to the scale of the system.

The D3186 outputs 12 different signals, providing comfortable measurement environment.

■ Variable Duty Cycle of Data Output Waveform

If the output duty cycle of the DUT characteristics decreases, a signal compensated by increased duty cycle can be input. It is also possible to decrease the duty cycle of the PPG output to evaluate DUT characteristics.

50 Ω Output Impedance

The D3186 employs a differential amplifier with 50 Ω back termination, allowing it to retain stable output impedance of 50 Ω both in high- and low-level output conditions. Even if an optical device such as a laser diode which may lead impedance mismatching is connected, waveform deterioration caused by signal reflection due to impedance mismatching is minimized.

Output Burst Signal

When SDH and FDDI frames are generated from a PPG (pulse pattern generator) or when long-distance round-trip testing is performed, burst signal output is required. With ADVANTEST's PPGs, burst signal can be output only by feeding an external gate signal.

■ Built-In Clock Source (Option)

In 12-GHz/12.5GHz band, remarkably high purity (high quality) signal is required as clock source for BERTS. In transmission system testing, it is necessary to connect the signal to the clock source which is prepared as system clock.

Specifications	
Internal Clock (optional):	
Frequency range : 150 MHz to 12 GHz (Option 10)	
150 MHz to 12.5 GHz (Option 13))
External Clock:	
Frequency range : 150 MHz to 12 GHz	
150 MHz to 12.5 GHz (Option 72))
Main unit operating frequency range	
: 150 MHz to 12 GHz	、 、
150 MHz to 12.5 GHz (Option 72))
DATA, DATA output:	
Amplitude: 0.5 to 2.0 V_{P-P}	
Offset: +2.0 V to -2.0 V (referenced to high level)	
Load impedance: 50 Ω Termination: GND mode, -2-V mode, and AC mode	
CLOCK1, CLOCK1 output:	
Amplitude: 0.5 to 2.0 V_{P-P}	
Offset: +2.0 to -2.0 V (referenced to high level)	
Load impedance: 50 Ω	
Termination: GND mode, -2-V mode, and AC mode	
CLOCK2:	
Amplitude: Max. 1.0 V _{P-P} fixed (AC coupling)	
Output patterns:	
PRBS (pseudo random pattern): 2 ^N -1, N = 7, 9, 10, 11, 15	, 23, and 31
WORD (programmable pattern): Max. 8-Mbit long	
SDH/SONET pattern: Max. STM-64/OC-192	
Trigger output:	
1/32 clock, pattern	
Auxiliary output:	
Data: 1/4 rate, 4 outputs	
Clock: 1/4 rate, 1 output	
1/2 rate, 1 output	
External storage devices:	
FDD: 2DD, 2HD (MS-DOS format)	
Options:)
OPT3186+10 : Clock source (150M to 12GHz) (Built-i	
OPT3186+10A : Clock source (150M to 12GHz) (Built-i	n)
(Installed at the factory) OPT3186+13 : Clock source (150M to 12.5GHz) (Built	t in)
OPT3186+13A : Clock source (150M to 12.5GHz) (Built	
(Installed at the factory)	111)
OPT3186+15 : Data Output $(0.5V_{p,p})$ to $3V_{p,p}$)	
OPT3186+15A : Data Output $(0.5V_{p-p} to 3V_{p-p})$	
(Installed at the factory)	
OPT3186+72 : Main unit operating frequency range (150M	(to 12.5GHz)
OPT3186+72A : Main unit operating frequency range (150M	
(Installed at the factory)	,
OPT2196, 70 Mixed pattern concretion function	

OPT3186+70 : Mixed pattern generation function

New 12.5Gbps Error Detector for SDH/SONET

D3286

- SDH/SONET frame synchronization suitable for system evaluation
- Error detection with area specification effective for SDH frame and ATM cell measurement
- Burst data measurement effective for Round-Trip test
- Auto search function which adjusts the most appropriate timing and voltage
- Monitor output of data and clock
- FD drive for storing measurement results and setup data
- GUI environment realizing easy and legible operating environment



D3286 Error Detector

To accommodate transmission of large-capacity information in the coming multimedia generation, ultra high-speed digital telecommunications networks are being constructed.

For evaluation and analysis of O/E and E/O modules and ultra high-speed logic devices used for multiplexers and repeaters for telecommunications systems, a signal source with high speed and high quality is necessary.

D3186 Pulse Pattern Generator/D3286 Error Detector offers excellent waveforms with high speed and high quality and diverse error detecting functions in an operating frequency range from 150 Mbps to 12.5 Gbps.

In addition, with the 8 M-bit large capacity memory and ADVANTEST's unique frame pattern generation function, D3186/D3286 is a new generation of error performance test system which is compatible with STM-1 (155.52 Mbps) to STM-64 (9.95 Gbps) in SDH/SONET.

■ SDH/SONET Frame Synchronization Suitable for System Evaluation

With SDH/SONET equipment, frames are recognized by means of the synchronization pattern described on the SOH (section overhead).

D3286 error detector mounts the circuit for recognizing the frame synchronization signal and has the capability to set not only SDH/SONET frames but also FDDI, ATM frames and arbitrary synchronization patterns, allowing frames to be synchronized with user-specific frame patterns.

Burst Data Measurement Effective for Round-Trip Testing

In long-distance round-trip testing, inter-satellite digital transmission testing and burst data (non-continuous data) are measured. Therefore conventional error detectors cannot be used. For easy measurement of burst data, D3286 error detector is provided with the internal gate and external gate measurement modes.

■ Error Rate Measurement Function with Area Specification, Effective for Measurement of ATM Cell

The measurement function with area specification of D3286 makes it possible to recognize whether the error occurs on the SOH or payload (in error measurement on SDH/SONET frames); measure errors within the specified cells (in error measurement on ATM cells).

New 12.5Gbps Error Detector for SDH/SONET

Creations

D3286

Automatic Adjustment to the Aimed Voltage at Optimum Timing with Any Mark-Space Rate and WORD Pattern

The auto search function allows D3286 to adjust to the aimed threshold voltage at optimum timing with any mark-space rate and WORD pattern, even if an error exists. In addition, GPIB interface makes it possible to read the voltage value, reducing the time for automatic measurement and evaluation.

Detailed Analysis of Error Measurement Results

The error measurement result classification function which classifies the result into omit error and insert error, displays them and makes it easier to recognize the tendency in error occurrence of the system and device under adjustment. For example, determine whether the amount of bias is appropriate or not. This function is evaluated as powerful and effective function at development, inspection sections and production lines.

■ Monitor Output of Input and Clock Data Effective for Evaluation of Jitter and Waveform Quality

During bit error measurement, by observing waveforms of the device under measurement without disconnecting the cables, waveform quality can be checked and the amount of jitter measured.

The monitor output can also be used as a signal to the clock generation circuit and is effective for O/E converters and OR devices.

■ Simple and Convenient Operating Environment with GUI (Graphical User Interface)

To allow the user easy concentration on the desired functions, D3286 configures graphical operating environment on the monitor of a personal computer.

Mouse-oriented operation and effective screen configuration make it easier to perform key selection without mis-operation.

Built-In FDD for Storing Measurement Results and Setting Data

D3286 mounts a floppy disk drive for storing measurement results and settings (measurement conditions).

Clock input:	
Frequency range: 150 MHz to 12.5 GHz	
Data input:	
Frequency range: 150 Mbps to 12.5 Gbps	
Sensitivity: 100 mV _{PP} typ. (12 Gbps)	
50 mV _{PP} typ. (6 Gbps)	
Approx. 50 Ω	
Measurable patterns:	
PRBS (pseudo random pattern): 2^{N} -1, N = 7, 9, 10, 11, 15, 23 a 31	and
WORD (programmable pattern): Max. 8-Mbit long SDH/SONET pattern: Max. STM-64/OC-192	
Measurement functions:	
Bit error rate	
Bit error count	
Bit error interval	
Bit error-free interval	
Threshold EI/EFI	
Error performance (conforms to CCITT G.821)	
Frequency	
Measurement modes:	
Normal, external gate and burst	
Area specification and error bit location (error location fund	ction)
(optional)	
Timer modes:	
Single, repeat and untimed	
Synchronization modes:	1.)
Normal synchronization and frame synchronization (selectab Alarms:	ie)
DATA : Informs a bit error.	
Sound pitch varies with the amount of errors. ALARM : Informs CLOCK interrupt, frequency reduction,	
pattern-out-of-synchronization,	
frame-out-of-synchronization and power failure.	
Sound volume: Variable	
External storage devices:	
FDD: 2DD, 2HD (MS-DOS format)	
Options:	
OPT3286+70 : Mixed pattern generation function	
OPT3286+72 : Main unit operating frequency range	
(150M to 12.5GHz)	

For Evaluating the In-Service Transmission Quality of Long-Distance Optical Transmission System

D3281

- Wide dynamic range (Q=10 to 34 dB)
- Short measurement time (3 minutes or less)
- \blacksquare Adapts to various transmission speeds by plug-in unit
- Clock phase can be optimized by Search-Eye-Margin function
- Clock phase can be controlled up to ±400 ps by 1 ps resolution.
- Abundant information is displayed on the LCD



D3281 Q Monitor

For the realization of multimedia environment, higher speed and greater capacity transmission are required. To achieve these, optical fiber cables and optical amplifier are used to make large-capacity and long-distance transmission possible. In general, for evaluating the signal quality of digital telecommunication line, pulse pattern generator and error detector are used to measure error rate.

However, as signal quality is improved due to the development of optical telecommunications, the evaluation method by error rate has reached the limit from the viewpoint of measuring time.

To solve this problem, instead of conventional error rate, it was devised to define Q value derived from signal amplitude and noise amplitude characteristics as the index for the evaluation. D3281 Q Monitor is the measuring instrument which can evaluate signal quality of ultrahigh speed digital telecommunication line, in the range from 500 Mbps to 6 Gbps.

For the evaluation with pulse pattern generator and error detector, specific known signal is necessary, however, the Q Monitor is not restricted by signal pattern and can be used as an in-service monitor of transmission quality during actual communication.

- **On-line monitor function** By generating reference pattern from the object signal from optical communication cable, on-line monitoring is possible.
- Clock recovery function By installing the plug-in type clock generator, the Q Monitor adapts to various transmission speeds.
- Wide measuring range and short measuring time Dynamic range : 10 to 34 dB is realized. Measurement time : approx. 3 minutes per measurement

For Evaluating the In-Service Transmission Quality of Long-Distance Optical Transmission System

Specif	ications — D328
Measurement function:	Power: DC -48 V DC (-41 to -68 V DC),
Data rate : 0.5 to 6 Gbps	5 A or less
Measurement function: Q value	AC 100 / 120 V AC or 200 V/240V AC,
Bit error rate	50 to 60 Hz (250 VA or less)
Auto correlative bit error rate	AC operation requires external AC adaptor.
Clock frequency (Accuracy ± 100 ppm)	Power consumption: DC 200 W or less
Q value measurement:	AC 250 VA or less
Measurement range: 10 to 34 dB (using attached 0.7m input cable)	Outside dimensions: approx. 260 (H) \times 435 (W) \times 450 (D) mm
Accuracy: ±0.5 dB or less	approx. 250 (H) \times 424 (W) \times 255 (D) mm
(Refer to BERTS and Noise Attenuation Method)	(Without AC adapter, handle and legs)
Data pattern 0101, at Q=15.5 dB, 22 dB	Mass: 20 kg or less, 13 kg or less (without AC adapter, handle and
± 0.5 dB or less	feet)
(refer to ADVANTEST standard)	Options:
23 stage PRBS, at Q=22 dB	OPT.3281+10 2 data input
7 stage PRBS, at Q=34 dB	OPT.3281+10 2 data input OPT.3281+17 Clock recovery plug-in unit (4.9 GHz)
Repeatability: 0.1 dB or less Standard deviation	
	OPT.3281+18 Clock recovery plug-in unit (5.3 GHz)
Measurement time: 3 minutes or less repetition	OPT.3281+15 Clock recovery plug-in unit (2.4 GHz)
Error count :	OPT.3281+16 Clock recovery plug-in unit (2.6 GHz)
Count range: 0 to 1,844E19	OPT.3281+40 220, 240 VAC
Gate control: Internal gate (0.1 to 99.9 seconds)	
Start/stop through GPIB & RS232	
External gate signal	
(0 to -1 V, 50Ω to ground)	
Elapsed gate time: max. 9,999,999 seconds, 0.1 second step	
Input, connections :	
Input signal: 1 data input	
2 selectable data inputs (OPT3281+10)	
External clock input	
External gate input	
Data input:	
Input amplitude: 500 mVp-p ± 2 dB + noise, Offset ≤ 0.5 V	
Variable threshold level: -1 to +1 V / 0.5 mV step	
Termination : 50 Ω to ground, K type connector	
Return loss ≥ 20 dB, 500 MHz to 6 GHz	
\geq 10 dB, 6 GHz to 10 GHz	
External clock:	
Input waveform: sine, square wave (duty 45 to 55%)	
Input amplitude: 0.5 to 1.0 Vp-p (AC coupled)	
Termination : 50Ω to ground, K type connector	
Internal clock recovery plug-in unit :	
Frequency : $4.97664 \text{ GHz} \pm 20 \text{ ppm} (\text{OPT}3281+17)$	
5.332114 GHz ±20 ppm (OPT3281+18) 2.48832 CHz ±20 ppm (OPT3281+15)	
2.48832 GHz ± 20 ppm (OPT3281+15) 2.666057 CHz ± 20 ppm (OPT3281+16)	
2.666057 GHz ±20 ppm (OPT3281+16)	
Variable delay :	
Delay time : -400 to +400 ps/1 ps step	
Others : Measurement control function :	
Measurement control function :	
Phase adjustment for data and recovery clock or external clock	
(auto and manual), Threshold DC level for input data and	
reference data (auto and manual), Gate time, 2 data input	
selection (OPT3281+10)	
Display function:	
Linear / log Q value (maximum, minimum, average, standard	
deviation), digital display for error count, phase adjustment and	
other control status	
Remote control:	
GPIB and RS232: set and read out for all control functions, phase	
adjustment, and threshold DC level, output data of error count,	
Output data of Q value, Output data of Q internal information	
(BER vs, Vth correlation coefficient)	

Operating environment : Temperature 0 to +50°C; relative humidity 85% or less Storage environment : Temperature -20 to +60°C; relative humidity 85% or less

Optimum for Evaluation of Built-in DSU Terminal (U point: Ping-Pong)

D5115

- Supports evaluation of ISDN devices and switches and IMT-2000 base stations and systems
- Supports optimum U point interface for evaluation of communications devices with built-in DSUs
- Supports multi-interface, multi-channel simultaneous monitoring and simulation functions
- Supports bit error rate test function that enables evaluation of line quality and other characteristics
- Supports LAN data transmission with Windows 95
- Employs platform that can flexibly respond to user needs
- Graphical user interface enables easy operation
- Supports PPP, IP translation (option)



D5115 Multimedia Protocol Analyzer

Features

The D5115 multimedia protocol analyzer has the flexibility to support evaluation of ISDN devices, switches, PBXs, and communications devices with built-in DSUs (routers, terminal adapters, etc.) as well as base stations and system evaluation for the next-generation IMT-2000 mobile communications protocol.

The D5115 can be taken advantage of for a wide range of applications, including development, production, and maintenance thanks to flexible system configured to meet diverse user environments by using the unit with the interface and function modules. In addition, the D5115 features easy operation by making use of the popular GUI used in the D5112 ISDN protocol analyzer. Using the same data format enables use of the data retrieved with the D5112 as well as the simulation programs, ensuring effective employment of existing resources.

■ Up to four modules mountable

It can run monitor, simulation, and bit error rate test (BERT) functions simultaneously on multiple channels and multiple interfaces by selectively combining independent interface and function modules.

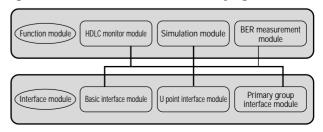
■ Simultaneous execution of multiple simulation programs The D5115 can simultaneously execute multiple simulation programs for selected interfaces. Sample programs stored in the main unit's hard disk can be easily modified to match user needs and abnormal communication sequences and error sequences can be easily reproduced.

This function also enables line switching function between selected interfaces.

■ Long-term monitoring function reliably captures

A 1G hard disk is integrated into the HDLC monitor function module to reliably capture communications errors (intermittent errors) for which the time of occurrence is unknown. Since this hard disk is divided into four partitions, four-channel simultaneous long-term monitoring can be achieved. D-channel can record approximately 900,000 frames (with a maximum frame length of 256 bytes).

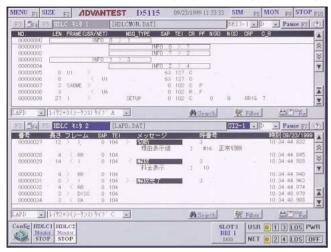
The D5115 can run multi-channel, multi-line long-term monitoring lasting up to several weeks depending on the amount of traffic. Moreover, data monitored over a long period can be efficiently analyzed using the search, filter, and other functions. Enables simultaneous quality evaluation of multiple lines The D5115 is capable of simultaneously performing multiinterface, multi-channel bit error rate tests to effectively evaluate line quality. The BER measurement function module allows BER measurement to be performed with up to six B channels (selected interfaces) at the same time when used in combination with the selected interface module (A simulation program is unnecessary). Simultaneous execution is also available for a maximum of four basic interfaces (D, B1 and B2 channels) with a single unit. This enables bit error tests to be carried out quickly for communication devices with multiple interfaces. When used in combination with the selected interface module, the simulation function module enables BER measurement using the selected B channel. (A simulation program is needed.)



Optimum for Evaluation of Built-in DSU Terminal (U point: Ping-Pong)

D5115

■ HDLC monitor screen (Layer 1 and sequence display)



Message builder screen (Enables easy creation and transmission of selected data)

IENU F1 SIZE F2	ADVANTEST	D5115	09/23/1999 1	2:22:32 SIM	FS MO	N F9 STO	P _{F1}
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Example of simulation function application (Enables implementation of line switching function between selected interfaces)



■ HDLC monitor screen (Japanese detailed display)

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Editor screen (Selected scenario preparation/ simulation program)

SIMMODE TE	TE simulation
LAYER 3	Layer 2 auto-execution mode
FUNC MAIN ()	Start of program
PH_ACT()	Layer 1 starts
WHILE (1)	Beginning of infinite loop
RECEIVE (0)	Wait until frame reception
IF RXMSG () ==5 THEN	If call setting (5) is received, THEN execute the following
LINKON ()	Layer 2 link starts
CRV=RXCRV () ¦H' 80'	Create send call number from receive call number
INSERT ("CONN",3,CRV)	Overwrite above line call number with send message reply (CONN)
SENDI ("CONN")	Send reply (CONN)
WAIT (100)	Stop program for 10 seconds
INSERT ("DISC",3,CRV)	Overwrite call number with disconnection (DISC) message
SEND ("DISC")	Send disconnection (DISC) message
END	End of IF statement
IF RXMSG () ==H'4D'THEN	If release (4D) is received, THEN execute the following
INSERT ("RELCOM", 3, CRV)	Overwrite call number with release completion (RELCOM) message
SENDI ("RELCOM")	Send release completion (RELCOM) message
EXIT	Exit from WHILE loop
END	End of IF statement
END	End of infinite loop
RETURN	End of program

Bit error measurement function (Simultaneous BER measurement of six selected channels of selected interface)

	有効	インタフェース	-	₹~ŀ'		开机	6	1/-1-		PRBS	/₩0	RD			
Ber1	V	PTI0-1	٠	NT	٣	B1	*	1536k		PRBS		PRBS7			
Ber2	7	PTI0-2	٠	NT	٣	B1	*	384k	٣	PRBS	٠	PRBS7			
Ber3	V	PTI0-2	٠	NT	٣	B7	+	384k	۷	PRBS		PRBS7			
Ber4		BRI1-1	*	NT	۲	Þ	٣	16k	۷	PRBS	*	PRBS7			
Ber5	8	BRI1-1	•	NT	٠	B1	¥	128k		PRBS	٣	PRBS7			
Ber6	Г	BRI1-2		NT	٣	B1	*	128k	¥	PRBS	*	PRBS7			
動方	 法 [i	時刻指定		2	-		-		-					a	<u>}</u>
	刻: 間:	10 / 01 時	Sec.	00	5	22	:	00 秒	00	-ù			Ľ	セッ	2 F

BER : Bit Error Rate

Optimum for Evaluation of DSU integrated terminal (U point: Ping-Pong)

D5115

- Specifications

Main unit	Protocols
OS : Microsoft [®] Windows 95 [®] operating system	
CPU : i486 [™] DX4 (100 MHz)	Layer 2: Q.921 (LAPD) Q.921-a, Q921-b, LAPB
	Layer 3: Q.931, Q-931-a, Q-931-b, X.25
Main memory: 32MB	Display format: Layer 1/2/3 individual display or simultaneous display
Built-in FDD: 3.5-inch (2 modes; 720kB/1.44MB)	Japanese sequence/detailed translated display/HEX display
Built-in HDD: 2.5-inch (1GB)	Storage capacity:
Serial terminal: RS-232 D-sub 9-pin	RAM; Approx. 2Mbytes/channel
Parallel terminal: Centronics D-sub 25-pin	HDD; Approx. 1Gbyte
External CRT terminal: Analog RGB mini D-sub 15-pin	Time stamp: Resolution 1ms (Max. recording duration: 127 days)
Mouse terminal: PS/2 type mini DIN 6-pin	Search function: Search by specifying time, frame, pattern, or error
Keyboard terminal: PS/2 type mini DIN 6-pin	Filter function: Layer 1 information, RR non-display, display of
PC card: JEIDA/PCMCIA compliant (type II \times 2 or type III \times 1)	specified TEI, SAP1, or call numbers.
Internal standard clock: Precision of ±5ppm	Audio monitoring function: A-law/u-law, 32k ADPCM/64k PCM, and
Display function: 10.4-inch (TFT color LCD with FL backlight, 640	selected single channel audio monitor using (3.5 headphone)
× 480 dots, 256 colors)	0 0 1 <i>i</i>
Power supply: AC100V to 240V, 50/60 Hz	Simulation function (D51130)
Dimensions: 355 (W) \times 250 (H) \times 170 (D) mm	Mode: When combined with the basic/primary group interface: NT
Mass: Approx. less than 6.4 kg (main unit only)	(network side)/TE (terminal side)
*Keyboard and mouse are sold separately. Customers are requested to either	When combined with the U-point interface: LT (switching office side)
supply their own or purchase from the list of Advantest accessories.	Line switching function: Function for switching between selected
	interface and selected B channel
Applicable interface	Loopback function: Loop-back of selected channel
Basic interface module (D51101):	Audio: Audio I/O to a selected channel with accessory headset
Interface:	(Note 4) included (A-law/u-law, 32k ADPCM/64k PCM)
I.430 (ISDN basic user, network interface layer 1 specification)	Bit error measurement: PRBS pattern, WORD pattern (16 bits)
I.430-a (Dedicated line user, network interface layer 1 specification)	LAPD function
Number of lines: Standard 1 line (max. 2 lines)	Applicable protocol: Q.921 (LAPD), Q931, X.25 (In addition to the
Operation mode: Monitor mode	above protocols, optional protocols are available in the HEX
Simulation mode; NT (network side)/TE (terminal side)	input mode)
Layer 1 detection: INFO 0,1,2,3,4,LOS (loss of synchronization)	LAPB function
Power supply polarity detection: OFF/normal/reverse	Applicable protocol: HDLC, X.25 (In addition to the above proto-
Wiring configuration setting: Short-range passive bus/Extended	cols, optional protocols are available in the HEX input mode)
passive bus/Point-to-point	cois, optional protocois are available in the TEX input mode)
End terminal resistance setting: OFF/50 Ω /100 Ω	BER measurement function module (D51140)
U point interface module (D51102):	Number of measurement channels: 6
Interface: TCC standard JT-G961	Channel rate (bit rate)
(ISDN basic access metallic link subscriber parent transmission method)	
(Ping-Pong method)	Channel 1 [bps]: 16K, 64K, 128K, 192K, 256K, 320K, 384K, 448K,
Number of lines: 1	512K, 576K, 640K, 704K, 768K, 832K, 896K, 960K, 1024K,
Operating mode: Monitor mode	1088K, 1152K, 1216K, 1280K, 1344K, 1408K, 1472K, 1536K
Layer detection: SIG status transition detection	Channel 2 to 6 [bps]: 16K, 64K, 128K, 192K, 256K, 320K, 384K
Power supply polarity detection: OFF/normal/reverse	Measurement pattern
Primary group interface module (1.5Mbps interface) (D51103):	PRBS: (2 -n-1 n=3, 4, 5, 6, 7, 9, 10, 11, 15, 17, 18, 20, 21, 22, 23, 25, 28, 20, 21)
Interface:	28, 29, 31)
I.431 (ISDN primary group speed user, network interface layer 1	WORD: Pattern length; 1 to 65,536bit
specification)	
I.431-a (Dedicated primary group speed user, network interface	IPV4 connection monitoring software (OPT5115+71)
layer 1 specification)	(PPP, IP translation software)
Number of lines: Standard 1 line	
Max. 2 lines (with OPT51103+01 installation module)	* Microsoft is a registered trademark of Microsoft Corporation in the United
Operating mode: Monitor mode	States and/or other countries.
Simulation mode; NT (network side)/TE (terminal side)	Windows is a trademark of Microsoft Corporation.
Layer 1 detection: USR; SYN, RAI, (AIS)	
NET; SYN, RAI, (AIS)	
$\mathbf{MET}, \mathbf{STIN}, \mathbf{MAI}, \mathbf{MIS}$	

Number of channels: Standard 2 channels, maximum 4 channels